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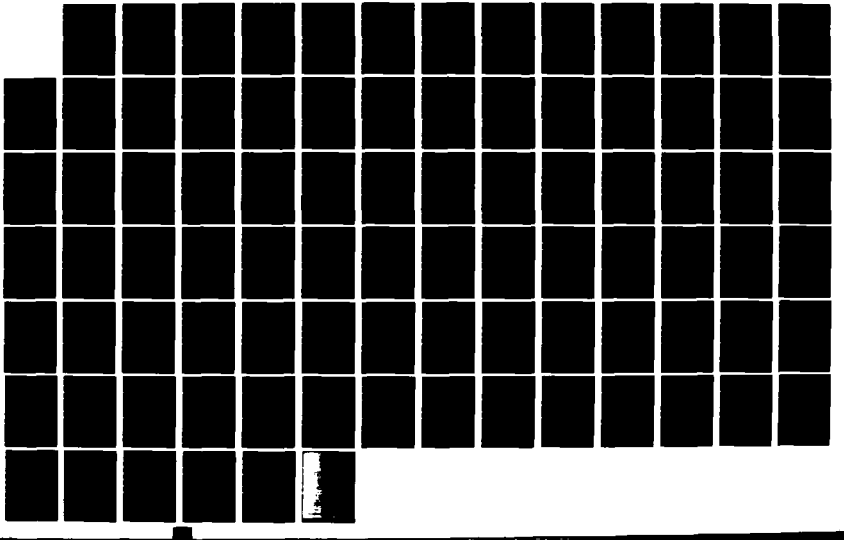

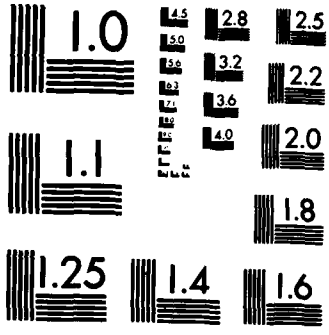

DNA 5915F

UPSET RESPONSE TESTING OF MSI INTEGRATED CIRCUITS

Boeing Aerospace Company
A Division of Boeing Company
P. O. Box 3999
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15 January 1982

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This study developed a standard test method for determining the upset response threshold of MSI integrated circuits. Differences in the upset response of internal logic cells were found that were caused by geometrical differences in the design and layout of internal transistors. An analysis method was developed and incorporated into the test standard which can identify these sensitive locations, providing a basis for selecting operating conditions for upset response testing.

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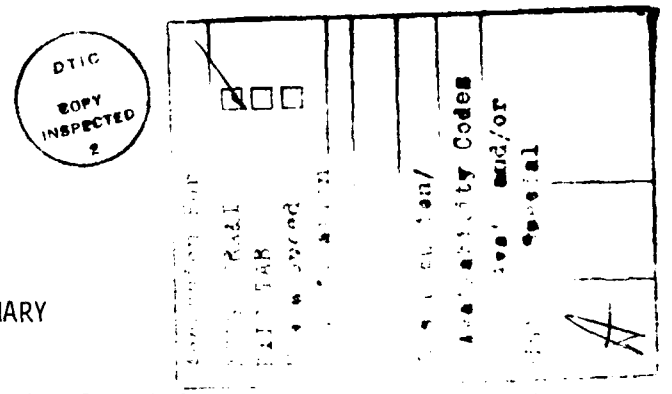

SUMMARY

In this study a test standard was developed for upset response testing of MSI integrated circuits when they are exposed to pulses of ionizing radiation. Internal response mechanisms were considered that can potentially cause certain internal locations to be more sensitive to transient upset than other internal locations. An analysis method was developed to identify these regions and select the most sensitive electrical conditions for radiation testing.

The test method was applied to five different TTL circuit types to compare the analysis approach with radiation test data. The selected circuits included junction-isolated circuits that were gold doped, junction-isolated circuits that used Schottky clamping, and special hardened circuits fabricated with a dielectric isolation process that also used Schottky-clamped transistors.

Two of the five circuit types had internal locations that were unusually sensitive to transient upset because of the geometrical design of internal transistors. The analysis method successfully identified these locations, and provided good quantitative agreement with the radiation test results.

The results of the study show that some MSI circuits have internal nodes that are unusually sensitive to transient upsets. A topological analysis is required in order to find these locations and specify the electrical test conditions for radiation testing. Without such an analysis, it is likely that sensitive operating modes will be overlooked, overestimating the radiation level at which the devices can safely be used.

A formal test method is included in the appendix that describes the procedure needed to analyze and test MSI devices when they are exposed to pulses of ionizing radiation. This procedure cross-references other applicable test standards, and specifies the equipment and apparatus required to test and analyze MSI integrated circuits.

The experimental work in the study was restricted to TTL devices, since they comprise the majority of MSI circuits. The analysis approach should be directly applicable to other MSI technologies such as CMOS and ECL. However, careful consideration must be given to response mechanisms that directly involve parasitic transistor gain which was not a factor for the TTL devices.

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INTRODUCTION

1-1 GENERAL.

The purpose of this study was to develop a standard test method for upset response threshold testing of MSI (medium scale integration) integrated circuits that are exposed to pulses of transient ionizing radiation. A formal test procedure was developed in the Mil-Standard format which is contained in the appendix.

The body of the report explains the technical approach in more detail than the formal Mil-Standard, and also demonstrates its application to five different circuit types. The results of the topological analysis are compared with experiment, and a general discussion is included about its applicability to other MSI digital circuit technologies.

1-2 ACKNOWLEDGMENTS.

Several people provided comments and suggestions that were incorporated in the final versions of the standard. These included Dr. E. A. Wolicki of NRL who also served as technical monitor; G. McLane (NRL); J. W. Harrity (IRT); E. E. King (Northrop Corporation); H. Eisen (HDL); H. Schafft (NBS); and T. Ellis (NSWC-Crane).

1-3 UNITS OF MEASUREMENT.

Metric units are used throughout this report. However, absorbed dose is commonly measured in rad (material) instead of Gray (material) as specified by current preferred metric units. Table 1 lists the conversion from conventional units to preferred metric units.

Table 1. Conversion factors for customary and standard metric units.

To Convert From	To	Multiply By
rad(material)	Gray (material)	1.000×10^{-2}

SECTION 2

BACKGROUND

2-1 P-N JUNCTION PHOTOCURRENT

2-1.1 Primary Photocurrent.

The excess carriers provided by transient ionization cause a photocurrent to flow across any p-n junction that is exposed to radiation. Under wide pulse conditions where time equilibrium is established, this photocurrent is given by the expression

$$i_{pp} = e \dot{\gamma} G A (W + L) \tag{1}$$

where i_{pp} = the primary photocurrent,
e = the magnitude of the electronic charge,
$\dot{\gamma}$ = the dose rate,
G = the carrier generation constant ($G = 4.2 \times 10^{13}$ $\frac{\text{e-h pairs}}{\text{rad(Si)-cm}^3}$ in silicon),
A = the junction area,
W = the junction depletion width, and
L = the diffusion length of minority carriers.

For nonequilibrium conditions, there will be a prompt component associated with the space-charge region of the junction and a diffusion term caused by the diffusion of minority carriers close to the space-charge boundary. For conditions where the pulse width is less than the minority carrier lifetime, the photocurrent is given by[1]

$$i_{pp} = e \dot{\gamma} G A \left\{ W + L \left[\text{erf } (t/T)^{1/2} \right] \right\} \tag{2}$$

where erf = the error function,
T = the minority carrier lifetime, and
t = the width of the radiation pulse.

Two other relations are useful when applying equations 1 and 2. First, the minority carrier lifetime is related to the diffusion length by the equation

$$L = \sqrt{D T} \tag{3}$$

where D is the diffusion constant. The depletion width is determined by the applied voltage and the doping levels on each side of the junction. For step junctions, the depletion width can be calculated from the relation[2]

$$W = \left[\frac{2\,\varepsilon\,(N_A + N_D)\,(V + \phi)}{e\,N_A\,N_D}\right]^{1/2} \tag{4}$$

where ε = dielectric constant

V = applied potential

ϕ = built-in potential ($\approx$0.8 V in silicon)

N_A = doping concentration on p-side, and

N_D = doping concentration on n-side.

Although more complicated expressions are needed for graded junctions, equation 4 can be applied to the collector-substrate and collector-base junction of integrated circuits.

The lifetime of silicon semiconductor devices varies from about 1 μs for non-saturating technologies, where no attempt is made to control the lifetime, to 10 ns or less for saturating switching devices that are heavily gold doped. Thus, for most gold-doped technologies equation 1 is adequate to describe i_{pp} even for narrow radiation pulse widths, while equation 2 must be used for non-saturating technologies such as Schottky TTL.

For applications in narrow pulse environments one is often more concerned with the lower integrated charge (effectively a drop in peak amplitude) than the explicit time dependence. Equation 2 can be used to calculate the effective charge reduction, given the nominal lifetime and radiation pulse width.

2-1.2 Secondary Photocurrent.

For transistors, the primary photocurrent may be amplified because of transistor gain, resulting in secondary photocurrent. The actual value of secondary photocurrent depends on circuit-related factors as well as the time dependence of both i_{pp} and the transistor switching characteristics. However, this photocurrent is always less than the limiting value provided by

$$i_{sp} = h_{FE}\,i_{pp} \tag{5}$$

where i_{sp} = secondary photocurrent,
h_{FE} = the common-emitter current gain, and
i_{pp} = the primary photocurrent of the base-collector junction.

For most digital circuits a simple hand calculation can be used to calculate the primary photocurrent needed to exceed the input logic threshold.

For integrated circuits, secondary photocurrents must be considered for parasitic as well as normal transistors. Most modern digital IC's use buried layers to reduce the parasitic transistor gain to very low values. This allows their secondary photocurrent to be ignored. However, the primary photocurrents associated with parasitic junctions are still important, as discussed in the following section.

2-2 CONSTRUCTION AND TOPOLOGY OF INTEGRATED CIRCUITS.

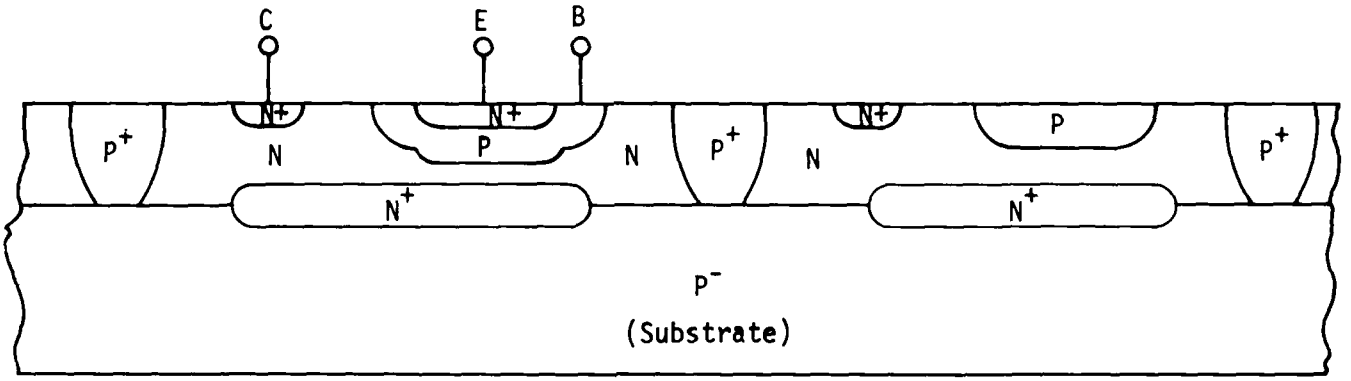
2-2.1 Junction Isolation (J.I.).

The overwhelming majority of integrated circuits are fabricated on a common substrate, using reverse-biased p-n junctions to maintain isolation between active circuit components. The presence of this parasitic isolation junction has a pronounced effect on the transient radiation response because the radiation-induced photocurrent associated with the substrate is much larger than that of other p-n junctions within the circuit.

A cross section of a typical bipolar logic circuit is shown in Figure 1. The substrate is lightly doped p-type silicon ($N_A \sim 10^{15}$ cm^{-3}). Buried layer (n+) regions are formed, and then an n-type epitaxial layer is grown over the entire surface. The purpose of the buried layer is twofold: it lowers the series collector resistance and also reduces the gain of the parasitic substrate transistor. The latter point is extremely important for transient ionization analysis since it virtually eliminates secondary photocurrent from this parasitic transistor.*

A subsequent p+ diffusion is used to form isolated n-regions for individual components. A p-type diffusion within the n-regions forms the base region of transistors; the base diffusion also is used to form resistors, as shown in the figure. An emitter diffusion completes the basic fabrication process.

*This buried layer is not present at the input protection diodes used in CMOS circuits and therefore parasitic transistor actions must be considered in detail when analyzing their transient ionization response.



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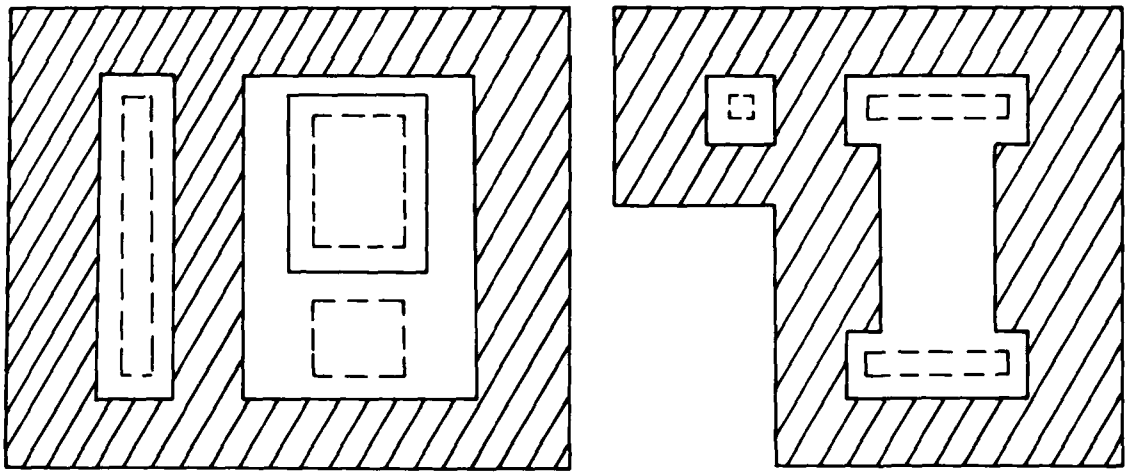


Transistor

Resistor

Top View

Figure 1. Cross-section and top view of typical components used in a junction-isolated TTL circuit.

The photocurrent of the collector-substrate junction is extremely large, due to its large area and the light substrate doping, which increases the junction depth ($W \sim 1/\sqrt{N_A}$, from equation 4). This junction surrounds every transistor and resistor within the circuit, and has an area that is only slightly smaller than that of the entire chip (the isolation diffusions occupy about 10% of the chip area). This large photocurrent tends to dominate the radiation response, even though secondary photocurrent is usually not involved.

Another factor that is important is lifetime. Older integrated circuits used gold doping to reduce the lifetime to levels below 10 ns, and their primary photocurrent time response was extremely fast. Newer technologies use Schottky clamping, forming a Schottky diode by extending the base metallization region over the collector. This eliminates the electrical requirement for gold doping because the lower forward voltage drop of the Schottky diode keeps the transistor from saturating. However, without gold doping the lifetime in the collector and substrate regions is ≈ 1 μs, with a corresponding equilibration time for primary photocurrent.

2-2.2 Dielectric Isolation (D.I.).

It is possible to eliminate the parasitic isolation junction by using a more complex, expensive process that results in dielectric isolation. This process uses the anisotropic etch properties of (1 0 0) silicon to form a V-shaped channel of known depth. Oxidation of these channels then provides dielectric isolation between n-type regions. Figure 2 shows a cross-section of a transistor fabricated with this process. Mechanical lapping is required in order to remove the n-epitaxial material that extends beyond the anisotropic etch depth. The collector tub depth varies across the wafer because the lapping is never exactly parallel to the other surface. Because of the many additional processing steps, the yield of D.I. devices is usually much lower than J.I. processes, and consequently it is seldom used for commercial devices. However there are some applications where superior electrical performance justifies its use. The elimination of the parasitic isolation junction provides obvious advantages in hardening devices in the transient ionization environment, so that D.I. construction is often used for special radiation-hardened circuits. A further advantage of dielectric isolation is that it eliminates latchup, provided that only one active component is placed in each isolated collector tub.

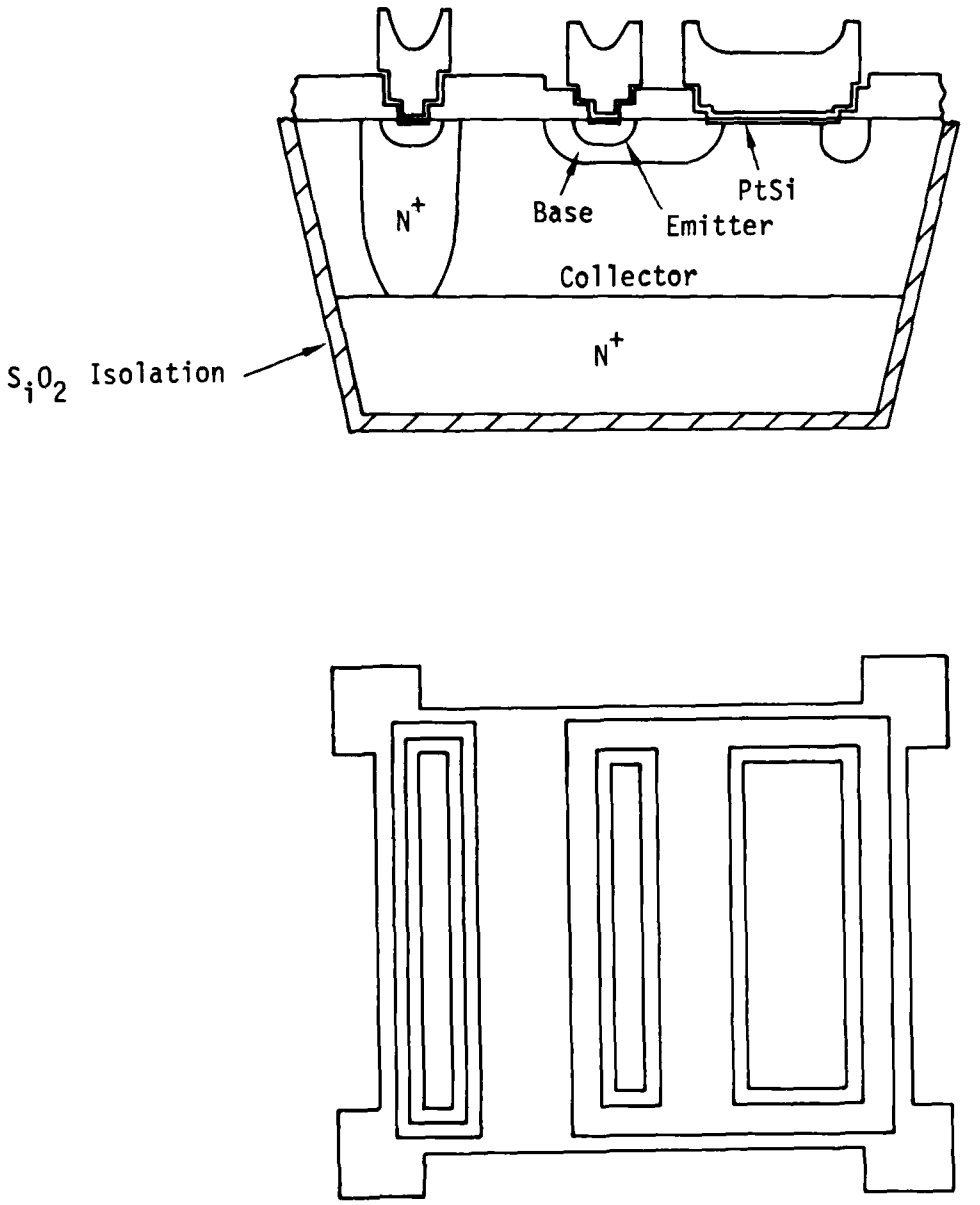


Figure 2. Cross-section and top view of a dielectrically-isolated transistor.

2-3 UPSET RESPONSE MECHANISMS IN TTL CIRCUITS.

The simple NAND gate illustrated in Figure 3 provides insight into the relative importance of various response mechanisms in TTL integrated circuits. For a junction-isolated gate, one finds experimentally that the lowest upset response threshold occurs in the high output state. The transient response exceeds the 400 mV noise margin in the range 2-4 x 10^8 rad(Si)/s for standard power, gold-doped TTL gates. Four mechanisms can potentially cause high-state transient upset:

1) substrate photocurrent of Q_2 through R_2 (this is transmitted directly to the output by Q_3, which operates as an emitter follower)

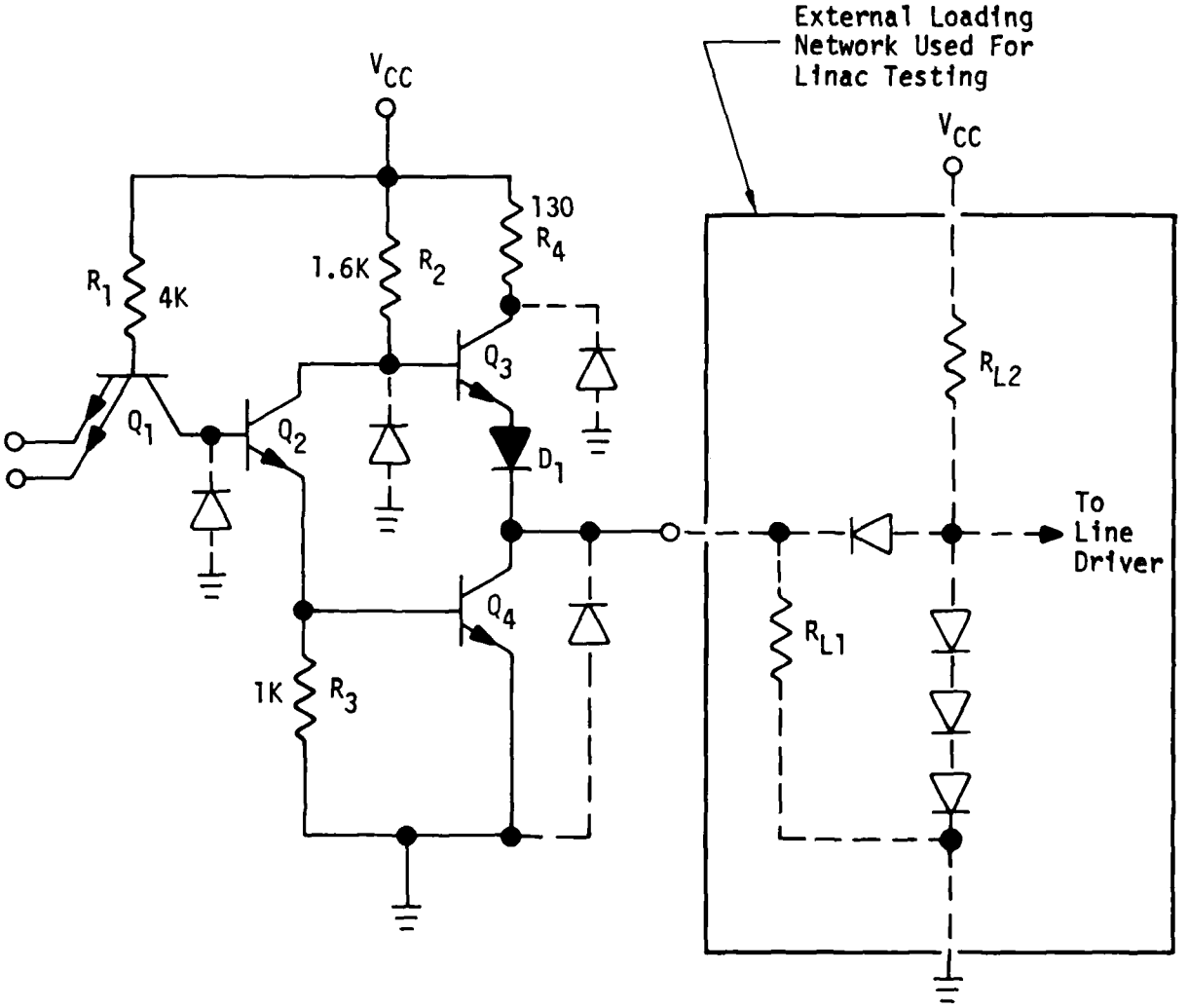
2) secondary photocurrent in Q_4

3) substrate photocurrent of Q_4 interacting with Q_3 and D_1 (the output voltage drops 120 mV for each tenfold increase in the emitter current of Q_3 because of the exponential relationship of V_{BE} and I_C).

4) secondary photocurrent in Q_2.

Typical chip layouts show that the ratio of the collector areas of transistors Q_4 to Q_2 is about three; we will also assume that the collector-substrate photocurrent of each transistor is about eight times that of its base-collector photocurrent. The substrate photocurrent of the output transistor is assumed to be 1 mA at 10^9 rad(Si)/s; this is based on a generation rate of $7 \times 10^{-9} \frac{\text{A-s}}{\text{cm}^2\text{-rad(Si)}}$ with a collector-substrate area of 1.4×10^{-4} cm^2, which is representative of gold-doped devices.

Table 2 shows the results of upset response threshold calculations for the above mechanisms. Clearly, substrate photocurrent is the dominant response mechanism. Secondary photocurrent does not become significant until levels nearly an order of magnitude above that at which substrate-related mechanisms cause upset. The relative ranking of these mechanisms depends on the resistor and junction area ratios. Unusual transistor geometries—such as an output transistor with an extremely large base area—may increase the importance of secondary photocurrent mechanisms. Large internal transistor geometries will also modify the results, and MSI circuits may contain such transistors.



Note 1: Substrate parasitic junctions shown as diodes (dashed connections).

Note 2: Loading network provides full fanout in both logic states.

Figure 3. Electrical schematic of an elementary TTL NAND gate.

Table 2. Upset response mechanisms for the TTL inverter.

Mechanism	Output Voltage Sensitivity	Photocurrent Region	Estimated Threshold [rad(Si)/s]
1	760 i_{PPS}	Q_2 (substrate)	2.7×10^8
2*	Hard failure at $\sim$ 1 mA	Q_4	$> 1 \times 10^9$
3	120 mV for 10X increase in current	Q_4 (substrate)	Combines with 1 to lower threshold $\sim$ X2 ($\sim 1.5 \times 10^8$)
4*	Hard failure at $\sim$ 1 mA	Q_2	2×10^{10}

*These two mechanisms depend on transistor gain and base body resistance, and are uncertain within a factor of two or more.

Since the most sensitive mechanisms depend on fundamental quantities—junction areas, lifetime, and resistor values—it is straightforward to apply this analysis to other variations of TTL circuits. For example, Schottky devices have a photocurrent that is approximately eight times larger per unit area. Their upset threshold will be eight times lower in a wide pulse environment (pulse width $\geq$ 1 μs), with lower factors for narrow pulses (see equation 2).

Other TTL circuit designs use different resistor values, resulting in different upset response thresholds. The two low power families—54L and 54LS—use resistor values that are nearly an order of magnitude greater. This increases their radiation sensitivity, although smaller transistor geometries are usually used because of the lower operating currents.

Although zero-state response mechanisms do not occur for simple gates, there are mechanisms that can cause such responses. The most likely mechanism is turn-off of Q_2 due to the substrate photocurrent of Q_1. In order for this to occur, the collector area of Q_1 must be a factor of 5 to 10 larger than the area of the typical input transistor used in SSI gates. In addition, Q_1 operates in the inverted mode with the input high, providing secondary photocurrent (this involves the inverted gain) that partially compensates for the substrate photocurrent. Thus, this mechanism is unlikely to occur, but could be important for devices with very large input geometries. MSI devices sometimes use input transistors as cross unders, diffusing emitters under the selected metallization run; this can result in much larger junction areas, and possible zero state failure.

For dielectrically-isolated circuits, the dominant response mechanism is almost always secondary photocurrent of the output transistor. Most D.I. devices are designed to be hardened to transient upset, and photocurrent compensation is often employed as a hardening technique. For these types of devices a simple topological analysis is of less value, because the circuit designer has already considered the simple geometrical factors that are so important for the J.I. technology. In most cases, the response threshold is determined by second order effects, such as photocurrent mismatches or internal body resistances that are generally beyond the capability of hand analysis. However, for unhardened D.I. structures the analysis method can be used in much the same way as for J.I. devices.

The TTL gate example shows the importance of different failure modes in determining the upset response. For junction-isolated devices, the dominant influence of substrate photocurrents allows simplifications when analyzing more complicated devices. The relative area of internal isolation regions is a key factor in establishing response mechanisms; these areas can easily be measured from a photomicrograph.

2-4 RESPONSE MECHANISMS FOR OTHER DIGITAL TECHNOLOGIES.

Although most MSI circuits are made with the TTL technology, ECL and CMOS circuits are also available. ECL logic circuits are also made using junction-isolation, and can be analyzed in much the same manner as TTL circuits. Substrate photocurrent is usually the dominant mechanism, and buried layers are used in their fabrication so that parasitic transistor gain is low.

CMOS circuits are fabricated differently, and have a much more complicated interaction with the substrate region because buried layers are not used. Many CMOS circuits exhibit latchup because of this substrate interaction. In many cases the latchup paths have involved the input protection diode network.[3] The relative areas of internal transistors are still important factors in determining the upset response threshold and may be used to identify sensitive internal regions. However, a complete solution to the CMOS upset problem must consider substrate interactions, which are generally beyond the capability of hand analysis.

Other mechanisms can also occur that are different from those encountered in simple gate structures. For example, Ellis and Kim have observed parasitic gain effects in I^2L LSI devices that occur in metallization cross unders.[4] These cross unders were only used on certain output lines. Overly optimistic upset levels could

result if the outputs with the cross unders were not included in the set of outputs that were monitored during radiation testing. This mechanism occurred because no buried layer is used in I^2L, resulting in high substrate transistor gains.

2-5 MSI UPSET TESTING CONSIDERATIONS.

2-5.1 Definition of Upset Threshold.

There are two basic types of MSI logic circuits. The first type consists of devices which rely only on combinational (static) logic and includes data selectors, multiplexers, most read-only-memories, and complex static logic chips. These devices have a fixed truth table which defines the relationship between the inputs and outputs that does not depend on dynamic pulse trains or clock references. For combinational devices, transient failure of internal logic cells will immediately affect one or more of the device outputs. Transient failures are detected by examining the outputs of the device during the radiation pulse; there is no need to perform elaborate functional tests after irradiation because functional operation is solely determined by the static input logic conditions. Geometrical or design factors (i.e., wire-or logic) may cause specific regions to have a low upset response threshold. The logic conditions used for radiation testing must include these regions in the logic path in order to find the correct operating conditions for the lowest upset threshold during radiation testing.

The second MSI device type consists of devices which rely on a sequence of dynamic pulse inputs to determine the output logic state (sequential logic). For these devices, internal flip-flops or registers store information, and transient radiation pulses may change the state of these internal logic cells. Since the output state depends on a complex sequence of input signals, these internal failures can only be detected by a functional test of the device outputs. This functional test requires a sequence of input pulses; the device outputs are tested for the entire series of input pulses and compared with the expected result from the device truth table to detect failure. This functional testing is required each time that a device is tested in a radiation environment. The functional test pattern can be very long for complex devices and adds considerable difficulty to the task of radiation testing.

The definition of upset is unambiguous when a nonrecoverable change in an internal storage resistor occurs (sequential logic), but is not well defined for transient responses at the device output which may occur for either type of logic circuit. The difficulty is that the noise immunity of a typical device in a radiation

test assembly is much greater than the worst-case noise immunity that applies in a real application. For example, with a 5 V power supply the output of a typical TTL device will have to fall from 3.5 to 1.5 V before it will affect the input of other circuits. However, the worst-case noise immunity is only 0.4 V; furthermore, system noise (caused by reflections from short unterminated lines, power supply transients, etc.) will consume most of this worst-case noise immunity. Consequently, in a real application a radiation-induced change of 50 - 200 mV can cause transient upset. This is an order of magnitude lower than the typical noise immunity. Since substrate-related mechanisms are proportional to dose rate, their response threshold drops by the same factor when the correct noise margin is used.

2-5.2 Total Dose Limitations.

In order to determine the upset threshold of a device in a given test condition, it is necessary to subject the device to a series of radiation pulses, testing the device for upset failure during and after each pulse. The radiation level is changed after each pulse until the failure level is bracketed. The final results are determined by successive approximation or interpolation. The number of pulses required depends on how close the radiation upset level is to the initial test level and also upon the accuracy needed. The minimum number of pulses is usually in the range of 3 to 10 pulses per input state condition. Even more may be needed for devices which have wide unit-to-unit variation in upset level.* Large numbers of radiation pulses are required to test a complex MSI part in all of its possible input conditions.

The total dose accrued during testing may introduce significant total dose damage to the device, which affects the end result, and is an unavoidable interference. Modern devices vary widely in total sensitivity. Furthermore, the significance of total dose damage cannot always be determined from the failure level associated with a given device technology. For example, Schottky TTL devices fail at levels well above 1 Mrad(Si).[5] Their electrical performance is only slightly affected by moderate gain changes, but the diffusion component of substrate photocurrent is

*In some cases it may be easier to test devices at several fixed levels. This is a faster test method, but the resolution is limited to the difference between successive radiation levels.

significantly reduced at levels far below the catastrophic circuit failure level. This will increase the apparent threshold for upset response, and illustrates the importance of understanding the mechanisms which cause the transient response.

For some devices, it may be possible to consider radiation testing in each possible input configuration. However, this approach cannot be used in general because of the large number of radiation pulses that is required. If the test method is to be usable for devices with high total dose sensitivity, the number of radiation pulses must be restricted to avoid interference from total dose degradation. This forces some means of restricting the test conditions for a generally applicable test method.

2-5.3 System Needs and Test Accuracy.

The importance of determining the precise level at which upset occurs is strongly dependent on the way in which a particular device is applied in a given system. For example, some tactical and avionics system have specifications which are much lower than the typical upset level of commercial MSI devices, and their testing needs are satisfied with a relatively coarse measurement. Their testing budgets are low; they are extremely concerned with testing costs and are willing to trade off cost and accuracy. On the other hand, strategic systems may have lower margins between the mean upset level and system survival level, and may also need accurate data in order to determine the statistical distribution of upset thresholds. The testing cost depends on the complexity and thoroughness of functional testing and the number of different logic states used for testing. The test method must allow some trade off between accuracy, completeness, and cost if it is to be generally useful.

2-5.4 Test Hardware.

MSI upset threshold testing requires elaborate test hardware, particularly for devices with complex functions. This test hardware must generate the appropriate input test patterns, synchronized with the radiation source, and must also compare the device outputs with the expected results. This hardware must operate satisfactorily in a noisy radiation environment, and requires careful checkout to make sure that functional errors are induced only by the devices response and not by instrumentation errors.

General purpose equipment can be used for less complicated devices. However, for more complex devices the fabrication and checkout costs become prohibitively high.

Specialized computer-controlled test systems are available which have elaborate functional pattern generation and comparison capability and can be programmed by high level computer languages. These flexible test systems eliminate much of the hardware development cost. However, a substantial effort is required to develop the initial test software and verify proper system operation.

SECTION 3

TECHNICAL APPROACH

3-1 OVERVIEW.

The approach used for the MSI transient upset response test method consists of a combination of circuit analysis and radiation testing which is then used to determine the states in which a specific circuit type is most sensitive to transient upset. Because the basic mechanisms that cause the transient response are intimately connected with the geometry and topology of the circuit, the analysis must generally include these factors. The analysis determines the relative photocurrents of internal transistors. Nominal values of gain and resistance are then used to find the regions that are most sensitive to radiation.

Sequential logic circuits are often most sensitive to upset when the radiation pulse occurs in coincidence with clock or internal circuit transitions. This is too difficult for hand analysis, and therefore supplementary radiation testing is used to determine the dynamic conditions in which the circuit is most susceptible to upset. The radiation tests can also be used to corroborate the analysis by comparing the upset threshold of different circuit conditions.

This test procedure addresses only transient upset, and does not consider latchup or photocurrent-induced burnout. Although the method should be applicable to any technology, the primary emphasis is on TTL circuits, since they comprise the majority of MSI devices.

3-2 DEFINITIONS.

The terms below require precise definitions in order to avoid confusion. Section 2-5.1 defines upset threshold, and also contains a more tutorial discussion of combinational and sequential logic circuits.

MSI Integrated Circuit. — An integrated circuit with a total number of internal components that is equivalent to the number of components contained in 15 to 100 gates. MSI stands for medium scale integration. Examples of MSI circuits include multiplexers, registers, counters, small memories and arithmetic logic units.

Combinational Logic. A digital logic system with the property that its output state at any time is solely determined by the logic signals at its input at the same time (except for small time delays caused by propagation delay of internal logic elements). Examples of combinational circuits include multiplexers and decoders.

Sequential Logic. A digital logic system with the property that its output signals at a given time depend on the sequence and time relationship of logic signals that were previously applied to its inputs. Examples of sequential logic include shift registers, counters and arithmetic logic units.

State Vector. A state vector completely specifies the logic condition of all elements within a logic circuit. For combinational circuits the state vector includes the logic signals that are applied to all inputs; for sequential circuits the state vector must also include the sequence and time relationship of all input signals. In this standard the output states will also be considered part of the state vector definition.

3-3 DEVICE RESPONSE CATEGORIES.

Before developing the details of the test method, it is important to examine the physical reasons that may cause the transient response to depend on the state vector of the circuit. Little evidence of state vector sensitivity has emerged from many years of testing SSI devices. Most devices exhibit only a narrow range of response thresholds, and the mechanisms that determine the response are well understood. There are also relatively few components in each logic path. It is generally assumed that abnormal devices will be screened out by the functional and switching tests that are done by the manufacturer.

The complexity of MSI circuits invalidates most of the assumptions that simplify the SSI problem, and there is a greater possibility of topological dependence of the failure modes. MSI responses may be state vector dependent because

1) the topology or design of the circuit causes one mode to be consistently more sensitive, or
2) random processing defects cause various regions of the device to have different radiation sensitivities.

The first mechanism is amenable to analysis, and is the mechanism that this test method attempts to identify. The presence of the second mechanism depends on the nature of the defects, the circuit design, and the functional and parametric tests that the circuit must meet. In general, this mechanism can only be identified by radiation testing the device in each state vector, which is usually inconsistent with cost and total dose limitations (see Section 2-5).

It is convenient to define three different categories of MSI device types which have different testing and analytical requirements. These categories correspond to the basic response mechansims as follows:

Category I: Devices which have straightforward internal design based on interconnections of standard logic blocks with no geometrical or circuit asymmetries. It is also assumed that the standard wide temperature range and burn-in testing requirements will reduce the probability of obtaining a device with abnormal response mechanisms to an extremely low value. For this type of device, testing the part under many different dynamic conditions with thorough functional testing after irradiation will give the same upset threshold as an abbreviated test. Simple logic circuits usually fall in this category because they involve simple replications of basic logic cells.

Category II: Devices for which certain modes, state vectors or topological locations are significantly more sensitive than others because of the electrical and/or topological design of the circuit. This behavior is consistent between devices from a given set of diffusion masks and processing steps and can be identified either by thorough complex testing or by careful analysis of the circuit design and topology. Mechanisms that can cause Category II responses include internal transistors with large junction areas, parasitic junction responses that result from chip layout, and the use of different logic cell designs for internal logic.

Category III: Devices which have lower transient threshold levels for certain internal cells because of random statistical variations in electrical parameters (i.e., leakage currents, resistance values, h_{FE}) or manufacturing tolerances (mask alignment, defect density, etc.) which are not screened out by the normal

testing and burn-in procedures. It is assumed that the probability of significant statistical variations in threshold levels is high enough to cause a serious problem in system applications. Examination of circuit function and topology can be used to distinguish between Category I and Category II devices, but cannot detect Category III devices. This kind of failure mode can only be found by elaborate, thorough testing of each device, or by tests of special test patterns that are designed to detect such failures. Mechanisms that can cause Category III responses include processing defects such as open resistors, mask misalignment, and emitter spikes that result in a lower turn-on threshold. Statistical variations in normal electrical parameters (such as h_{FE}) may also result in Category III responses. These statistical fluctuations are more important for MSI devices because of the larger number of components and the large number of logic paths, which tend to isolate the interior of the device from the terminals. In general standard electrical tests are less likely to weed out marginal logic cells because of this isolation.

The definition of these three basic response categories establishes the type of mechanisms that MSI testing can be expected to uncover. Along with the device response analysis, they provide a basis for selecting the minimum set of state vectors required for a meaningful test. They also provide a way of estimating the risk of overlooking sensitive failure modes when an abbreviated test method is necessary because of cost or total dose limitations.

Before discussing the analysis approach, it should be noted that existing upset response data shows that most MSI devices also fall into response Category I. Thus, the chances of encountering devices that have sensitive state vectors is relatively small. This seems reasonable for circuits that are largely made from logic cells that are similar to SSI gates, but is clearly not valid for MSI devices in general. Furthermore, this test data usually involves a very limited number of state vectors, and it is possible that sensitive modes have been overlooked for some devices.

3-4 ANALYSIS METHODS.

3-4.1 Topological Analysis.

The first step in the analysis is a visual examination of the device topology with a microscope or photomicrograph. Its purpose is to determine the relative areas of internal components, and also to check for layout asymmetries (particularly those involving parasitic junctions) that may affect the upset response.

Our experience with SSI devices usually allows the analysis to be restricted to a few components because one failure mechanism is expected to dominate the device response. For example, the response of the TTL gate discussed in Section 2-3 was clearly dominated by substrate photocurrent in the phase splitter transistor. Very large increases in the area of other transistors would have to occur in order for other mechanisms to become significant, and this can easily be checked by visual examination. In this case precise measurements of device areas are not required; the important point is to check for unusual component geometries. This assumes that the internal logic cells used in more complex devices are similar to SSI logic elements. Although this is usually the case, it should be verified as part of the topological analysis.

For junction-isolated devices, it is relatively easy to estimate the photocurrent generation constant per unit area, enabling a reasonably accurate calculation of the photocurrent and response threshold from the junction areas and nominal resistance values. The accuracy of the photocurrent calculation can be checked experimentally by calculating the expected photocurrent of the entire chip and comparing with experiment. A small correction must be made to allow for isolation diffusion and bonding pad areas.

For dielectrically-isolated devices (or J.I. devices that respond because of secondary photocurrent) it is more difficult to estimate the photocurrent because of its dependence on the collector tub depth which is not precisely known. Secondary photocurrent mechanisms also depend on internal body resistance values which are also difficult to estimate. Thus, the analysis method is quantitatively less successful for secondary photocurrent mechanisms. However, it is still effective in identifying large internal photocurrent regions, which is one of the most likely reasons for topologically-dependent response levels.

These analysis methods are limited to the steady state, although correction factors can be applied for the effective charge reduction of narrow radiation pulses (see equation 2). For most integrated circuits, not enough information is available about internal components to justify a transient analysis of the device radiation

response. Exploratory radiation testing is used to determine the most sensitive timing relationship between electrical input signals, such as clock or enable pulses, and the radiation pulse.

3-4.2 Functional Logic Analysis.

The selection of the particular state vectors that are to be used for radiation testing depends on a functional logic analysis as well as the topological analysis. The logic analysis requires familiarity with the functional operation of the specific circuit. For example, radiation testing of a memory circuit must include both the write and read modes; such circuits are usually most sensitive in the write mode because the write circuitry is active during the radiation-induced transient. No specific rules can be given for this analysis because of the limitless variations of MSI circuit functions. In general the circuit should be tested in all of its basic operating modes, but the number of input state vector variations and outputs that are examined can be restricted because of internal layout symmetries that are known from the topological analysis. For most MSI circuits it is relatively easy to select the basic operating modes. However, for devices with highly complex operating modes (such as an arithmetic logic unit) more emphasis may have to be placed on exploratory radiation testing to establish the correct state vectors.

3-4.3 Functional Testing.

For sequential circuits, radiation-induced changes in internal storage registers are detected by a functional test that occurs shortly after the radiation pulse. This functional test must be as complete as possible. For circuits with relatively simple functions, such as binary counters or shift registers, the functional test can simply be a bit by bit comparison of the output from an oscilloscope photograph. For more complex devices, some form of memory and comparison circuitry is needed because of the large number of bits that need to be examined. For example, functional tests of memory circuits can be made with simple logic systems that compare the device output with that of a reference memory. Figure 4 shows an example of such a functional test method for a memory circuit. Commercial equipment such as logic analyzers or semiconductor test systems can also be used for functional testing. Computer-controlled test systems are especially valuable for complex functions that are expensive to implement with custom hardware.

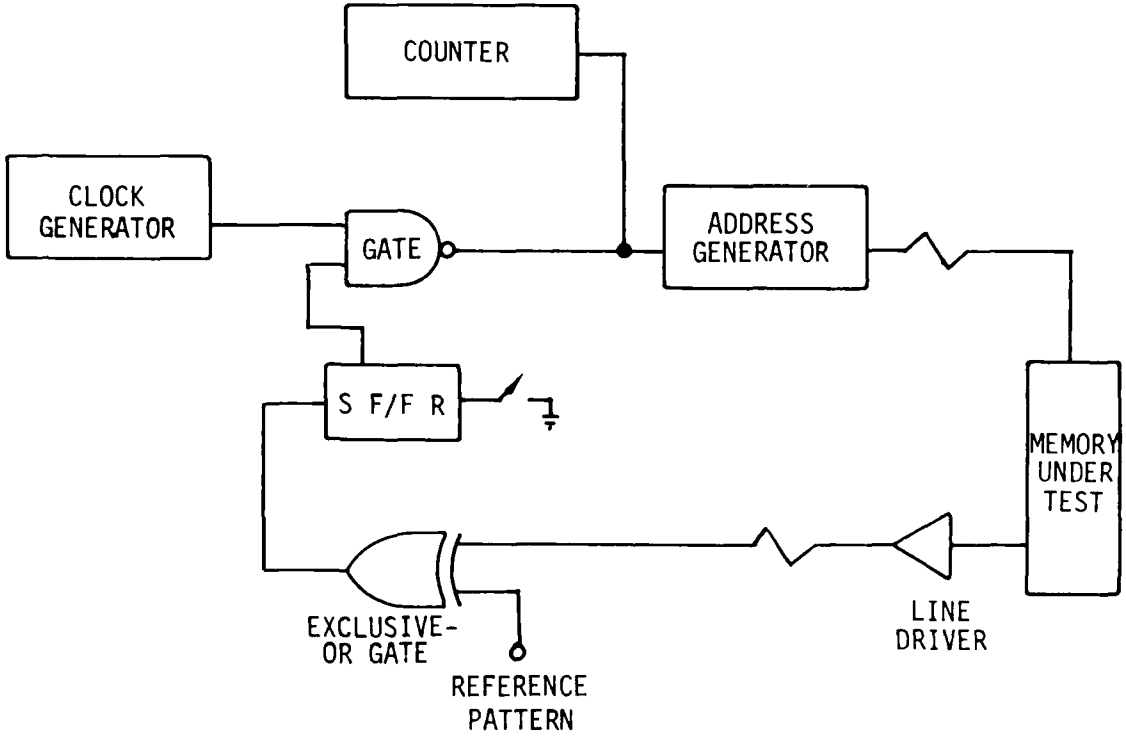


Figure 4. Example of functional test methods for random access memories.

3-5 RADIATION TESTING.

Exploratory radiation testing is done using a small number of expendable test samples to determine the most sensitive state vectors. The primary purpose of this testing is to identify the most sensitive position of the radiation pulse with respect to the pulsed input signals that are used to set up the device state vector. Even with expendable devices, only a limited number of permutations of state vectors can be used because of the time and facility cost. The state vectors and device conditions identified in the analysis step are the logical starting conditions for exploratory testing. It is important to compare carefully the radiation test results with the response that was anticipated by the analysis. A quantitative comparison of the upset response threshold with a calculated value can be used to substantiate the internal response mechanisms.

After the appropriate state vectors are determined, a test plan can be written for subsequent testing of actual samples. Because of the possibility of total dose damage, the test plan must carefully control the number of pulses that are used in determining the upset threshold. The following items should be included in the test plan:

1) Radiation source requirements (pulse width, type of simulator)

2) Specific state vectors used for upset threshold testing

3) Functional test requirements

4) Specific details of the test fixture (supply voltages, loading conditions)

5) Equipment specifications for upset response measurement

6) Procedure for determining the upset threshold by successive approximation

3-6 CIRCUIT SELECTION.

All of the circuits selected for this study were TTL devices. This technology was emphasized because the majority of MSI circuits utilize it. ECL circuits were not included because of their more limited use in military systems. CMOS circuits are available in several MSI functions, but their sensitivity to latchup, which is not addressed by this standard, forces a different emphasis. Until the CMOS latchup problem is eliminated, it is unlikely that many systems would be concerned about their upset response threshold. Other technologies such as NMOS and I^2L are not available in MSI functions, even though they are widely used for LSI designs.

Five different TTL devices were selected to demonstrate the application of the test method. Three of them were junction-isolated devices that are standard commercial designs, while the other two were special radiation-hardened circuits that use dielectric isolation. One of the D.I. circuits was functionally identical to one of the J.I. devices, allowing a direct comparison of these technologies. Table 3 below summarizes the essential features of the five circuit types.

Table 3. Circuits selected for demonstration of the test method.

Circuit Type	Description	Fabrication Technology	Manufacturer (Date Code)
54151	8-Bit Multiplexer	Junction-Isolated TTL	T.I. (8029)
54193	4-Bit Counter	Junction-Isolated TTL	T.I. (8105)
74LS670*	4x4 Register File	Junction-Isolated Low Power Schottky TTL	T.I. (8109)
477-1276	4-Bit Counter	Dielectrically-Isolated Low Power Schottky TTL	T.I. (7912)
477-1284*	4x4 Register File	Dielectrically-Isolated Low Power Schottky TTL	T.I. (7921)

*These two circuits were electrically equivalent to allow comparison of the two fabrication technologies.

SECTION 4

ANALYSIS OF SELECTED CIRCUITS

4-1 JUNCTION-ISOLATED CIRCUITS.

4-1.1 General Considerations.

Response Mechanisms.—From the general discussion of TTL response mechanisms in Section 2-3, the dominant response mechanism is expected to be the voltage drop of substrate photocurrent in the phase-splitter transistor (Q_2 in Figure 3) through its load resistor. Secondary photocurrent mechanisms are unimportant because of the differences in junction areas of the base-collector and collector-substrate junctions, along with the relative resistance values used in the logic cell design. The area of the output transistor would have to increase by at least a factor of 5 in order for the secondary photocurrent response to compete with the phase-splitter substrate photocurrent mechanism. This analysis assumes that internal MSI logic cells are similar in design to the familiar logic cells used in SSI devices, and it is important to verify this with the photomicrograph.

Substrate Photocurrent Calculations.—Substrate photocurrent can be calculated from first principle using equations 1 through 4. Although the exact values of lifetime and doping levels are unknown, the photocurrent varies as the square root of both, and hence nominal values are usually satisfactory for estimating photocurrents. Table 4 shows the results of photocurrent sensitivity calculations for gold-doped and Schottky devices assuming a substrate doping level of 10^{15} cm^{-3} and an applied voltage of 5 V. The lifetimes were assumed to be 10 ns and 1 μs, respectively for the two technologies. The calculations show that the diffusion-length contribution of the photocurrent is the most significant, even for the gold-doped devices.*

*Leedy, et al.[6] conclude that the depletion contribution dominates for gold doped devices because of the observed temperature dependence of the photocurrent. However, they do not explicitly calculate the diffusion contribution. Furthermore, their estimates of upset threshold are a factor of 2 lower than their experimental results, indicating that the diffusion contribution is about equal to the depletion contribution for their devices, which is in reasonable agreement with the above calculations.

Table 4. Substrate photocurrent sensitivity of junction-isolated TTL circuits.

Technology	Nominal Lifetime [ns]	Depletion Width [μm]	Diffusion Length [μm]	Calculated Sensitivity $\left[\frac{A\text{-}s}{cm^2\text{-}rad(Si)}\right]$	Measured Sensitivity $\left[\frac{A\text{-}s}{cm^2\text{-}rad(Si)}\right]$
Gold-Doped	10	2.6	6.3	6.0×10^{-9}	6.9×10^{-9} (54151) 6.2×10^{-9} (54193)
Schottky	1000	2.6	63	4.1×10^{-8}	5.1×10^{-8} (74LS670)

Experimental data for the three junction-isolated devices are also included in the table for comparison. These data were obtained by measuring the chip area, subtracting 15% to allow for isolation diffusion and bonding pad areas, and measuring the power supply current surge at a dose rate that was low enough to rule out the possibility of secondary photocurrent. There is surprisingly close agreement between the calculated and measured values. Note that the photocurrent sensitivity of the Schottky devices is nearly an order of magnitude greater than the gold-doped devices because of the long lifetime.

4-1.2 54151 8-Bit Multiplexer.

Response Analysis.—The 54151 represents a basic type of combinational logic circuit, and is fabricated with the standard gold-doped TTL technology. As shown in the schematic diagram of Figure 5, the internal circuitry is nearly identical to that used in elementary TTL gates. The one difference is the phase-splitter connection. A "wire-or" configuration is used, connecting the output of eight phase-splitter transistors to a single pull-up resistor. Since the dominant response mechanism involves substrate photocurrent at this node, this design feature is expected to have a large impact on the radiation hardness.

Examination of the topology of this circuit shows that the "wire-or" connection is obtained by diffusing eight separate base regions into a single collector isolated region. Figure 6 shows the geometry of this transistor; its area (3.6×10^{-9} cm^2) is about a factor of 7 greater than that of a single-collector

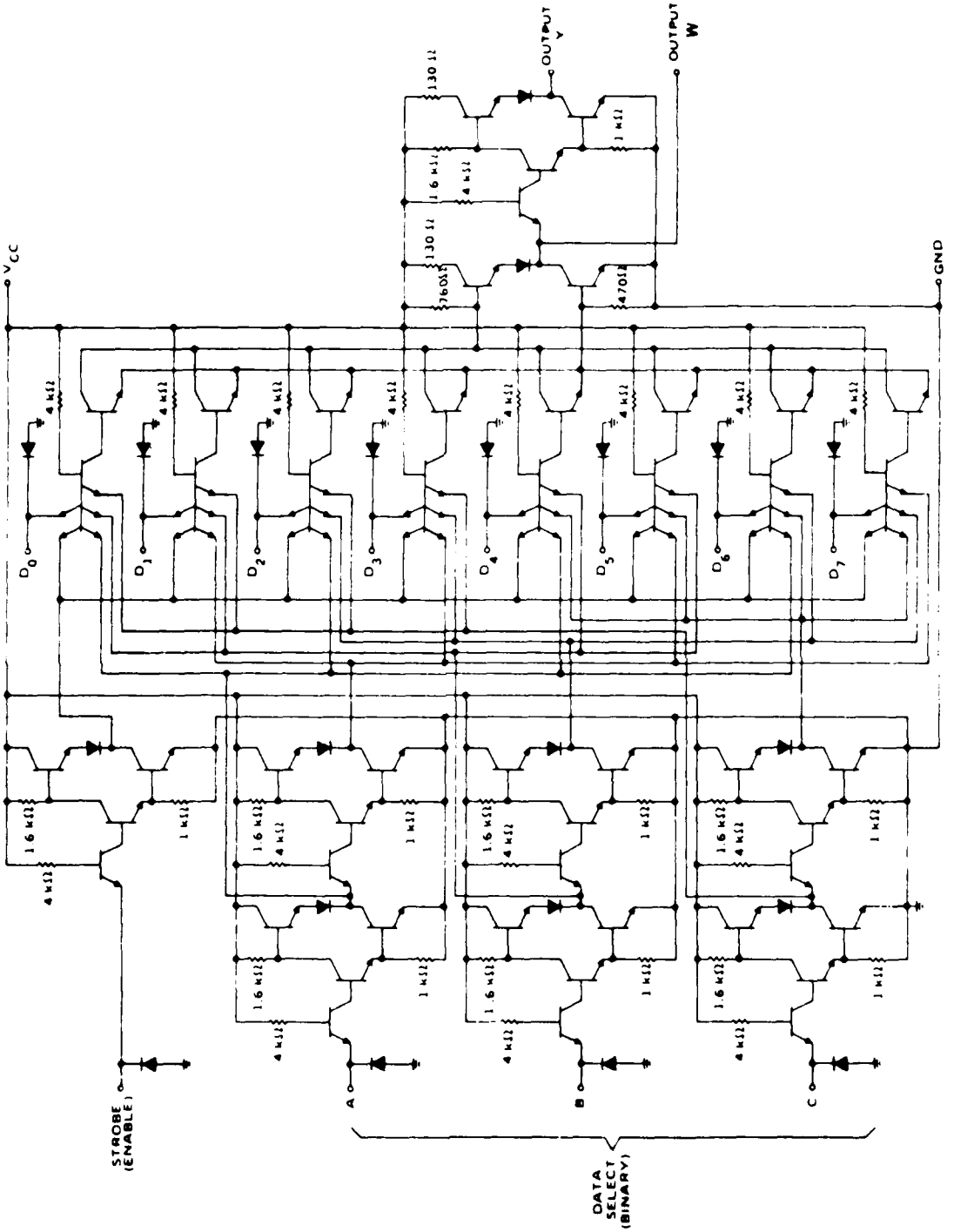
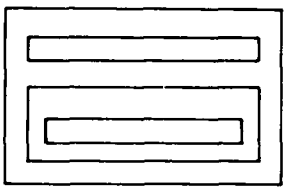
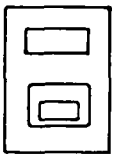


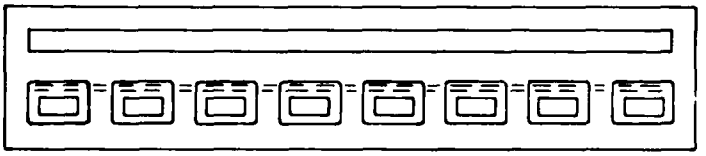
Figure 5. Circuit schematic for the 54151 8-bit multiplexer.



a) Output Transistor



b) Typical Phase-Splitter Transistor



c) "Wire-or" Connected Phase-Splitter Transistor (Eight Inputs)

Figure 6. Top view of various transistors used in the 54151 multiplexer.

transistor. Since the manufacturer used a lower pull-up resistor, the expected response of the "W" output is expected to be a factor of 4 higher than that of the "Y" output, which involves only a standard inverter.

State Vector Selection.—Since this is a combinational circuit, it is relatively easy to select state vectors for radiation testing. The symmetry of the internal design shows that all eight inputs are essentially equivalent, and radiation testing could be limited to one high state condition. This is also consistent with a functional logic analysis of the circuit. However, the outputs are substantially different in their sensitivity to transient upset because of the internal design difference. Output "W" must be included in the outputs that are measured; if only output "Y" were included, the upset response threshold of the circuit would be seriously overestimated.

Although the analysis shows that only one state vector is required, it is relatively easy to measure both outputs and also select several inputs. This larger set of state vectors was used for radiation testing.

Functional Testing.—Since the 54151 is a combinational circuit, there are no internal storage elements and functional testing is not required to determine the upset level. However, a functional test is needed to verify proper biasing and operation of the circuit. Because of its simple logic function, this is easily implemental using general purpose pulse generators and oscilloscopes to manually verify correct functional operation.

4-1.3 54193 Counter.

Response Analysis.—The 54193 is a 4-bit up/down counter that is a basic type of sequential logic circuit. A block diagram of this circuit is shown in Figure 7. From this diagram, the internal logic is composed of basic logic gates along with four internal flip-flops that store the binary count. Based on the logic design, there are no obvious asymmetries to aid in the selection of a specific state vector. There are two possible response modes: recoverable transient signals that are similar to the response of a simple gate, and non-recoverable counting errors. Inspection of the logic diagram shows that the transient mechanism is simply due to the output stage of the flip-flop, while the change-of-state mechanism could be caused by the transient response of the logic gates or the flip-flops themselves. Since the on-chip noise immunity is much greater than the worst-case value used to determine output transient failure, the threshold for counting errors is expected to be a factor of 3 to 5 higher.

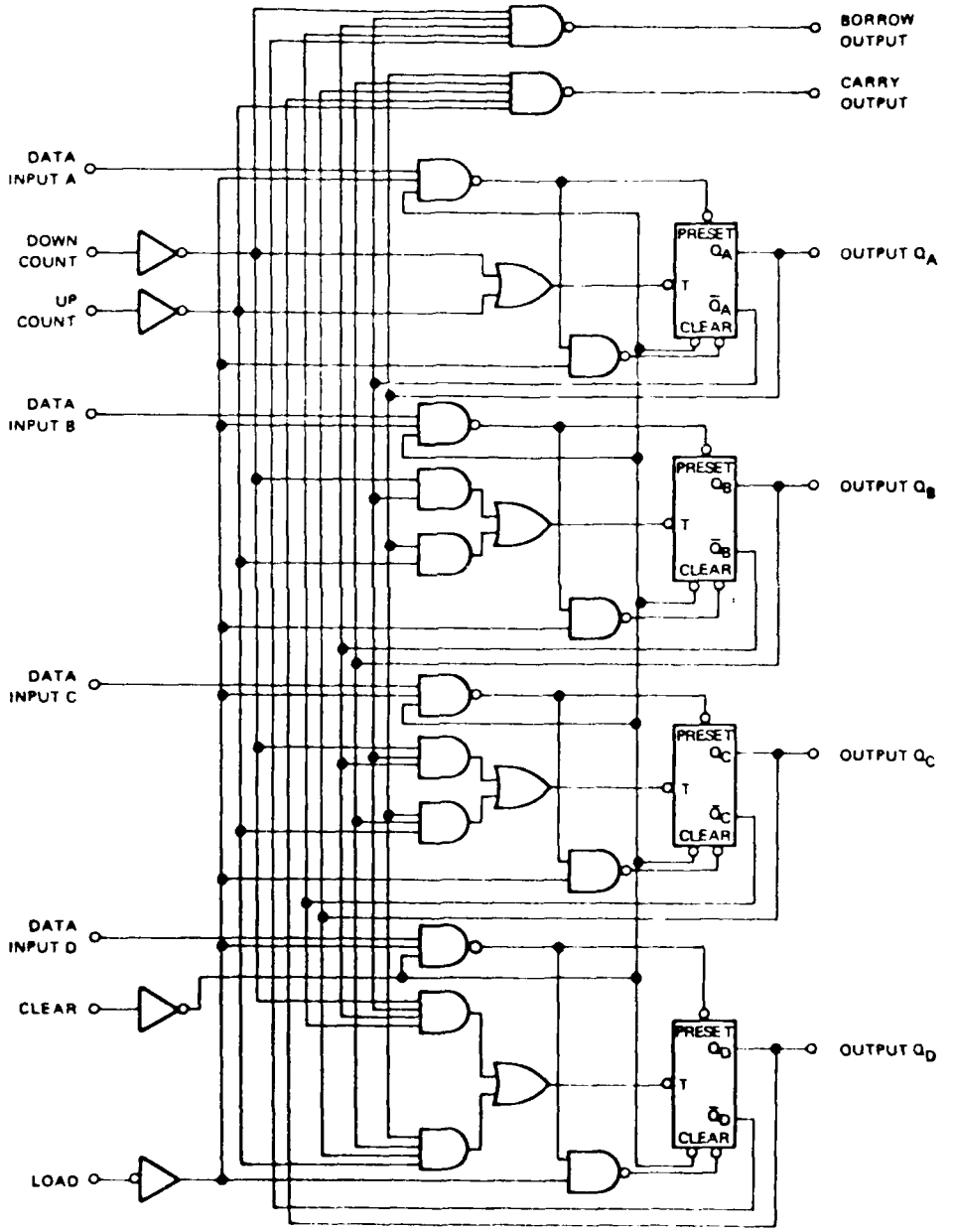


Figure 7. Logic diagram for the 54193 counter.

Examination of the internal transistor geometries shows that "wire-or" logic is used for the internal OR gates. The geometry of selected transistors is shown in Figure 8. The normal OR gate phase-splitter transistor has an area that is about twice that of an inverter phase splitter; in addition one of the phase splitter transistors has a third base diffusion that is not connected in the circuit. This transistor is contained in the OR gate used to drive the Q_D output (most significant bit). Therefore this is the condition in which the device is most sensitive.

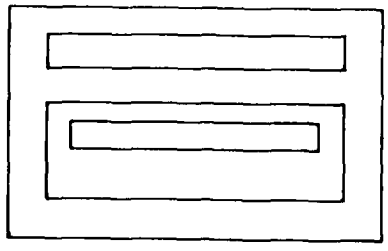
Figure 8 also shows that the internal input transistors have large areas. The emitter diffusion is selectively placed to select one (or more) of several metallization runs; the remaining area is used as a cross under. However, the SSI gate analysis shows that this is not a significant failure mode.

State Vector Selection.—From the response analysis, the MSB transition is the most sensitive internal point, so that the device should be most sensitive to radiation when the radiation pulse overlaps the high-to-low transition of the MSB output. Although this state vector is the most sensitive, it is easy to vary the position of the radiation pulse to experimentally find the most sensitive timing relationship. Based on the topological analysis, the sensitivity should be the same in either the up or down counting mode.

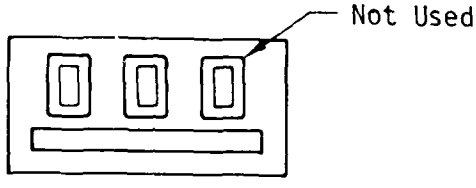
Functional Testing.—Because the 54193 is a sequential logic circuit, functional testing is the only way to determine count loss. The functional test consists of a sequence of clock pulses and input signals, monitoring the output of all four bits to determine counting errors. The clock and input signals must be synchronized with the radiation pulse.

4-1.4 74LS670 Register File.

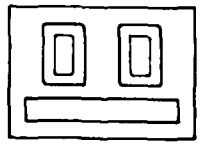
Response Analysis.—The 74LS670 register file is also a sequential logic circuit, and a logic diagram of this circuit is shown in Figure 9. This device is fabricated with the low power Schottky technology, resulting in much lower upset threshold responses because of the high photocurrent and high resistance values. Functionally it introduces an added complication because the outputs are designed to have a high impedance condition (tri-state) unless the G_R output is low. Transient failure in the tri-state condition cannot be well defined unless the details of the application are known.



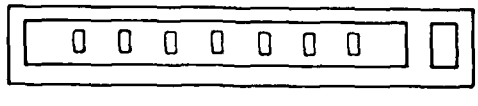
a) Output Transistor



b) Two-Input "Wire-or" Phase Splitter
(extra base diffusion not connected)



c) Standard Two-Input "Wire-or" Phase Splitter



d) Multiple Emitter Input Transistor

Figure 8. Top view of various transistors used in the 54193 counter.

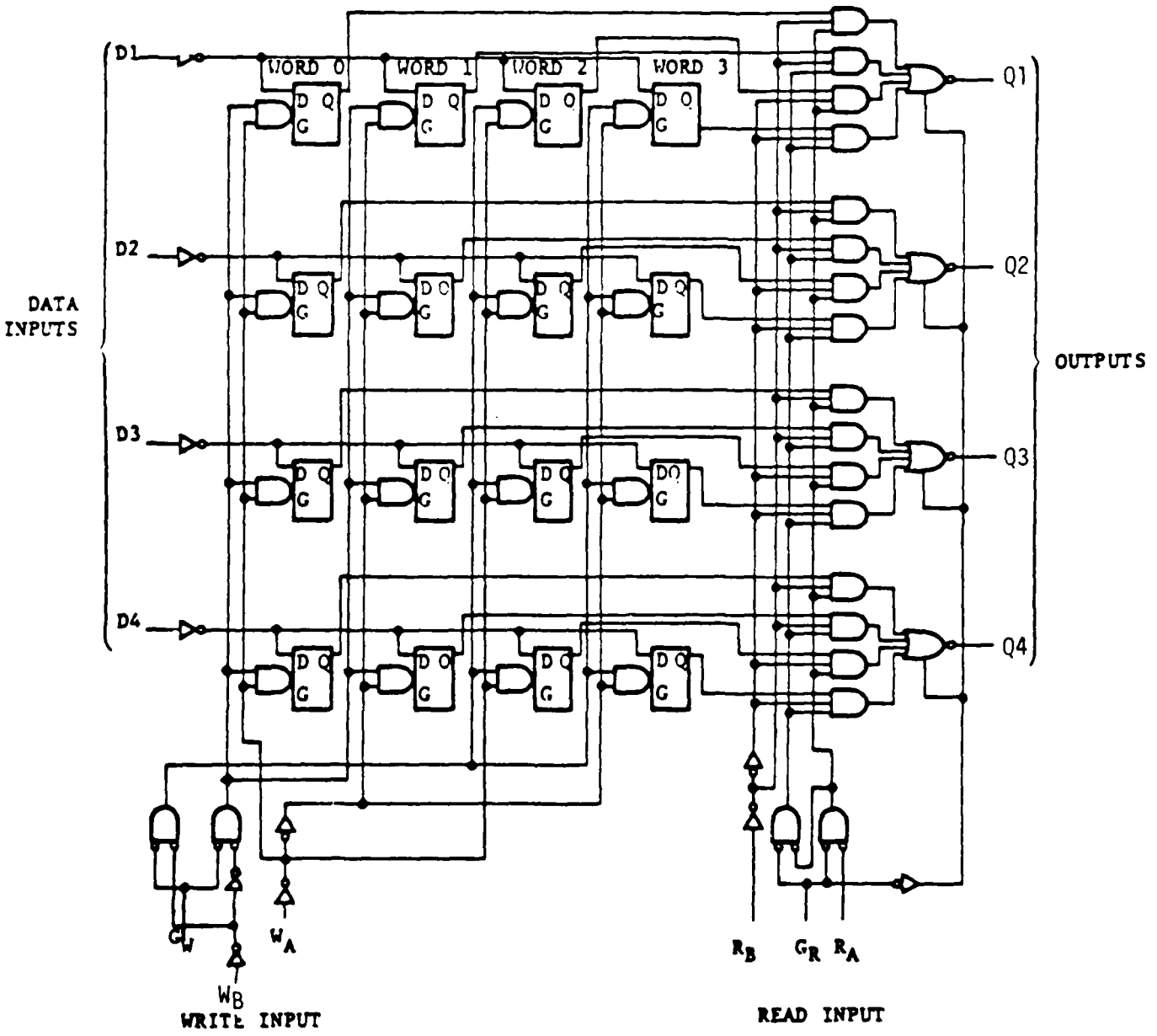


Figure 9. Logic diagram for the 74LS670 and 477-1284 register files.

The logic design is symmetrical, and since the output stage inverts, high-to-low changes in internal memory will be inverted so that the output is expected to show zeros becoming ones.

Topological examination shows that the flip-flops use essentially a standard SSI logic design. The output transistors and the 4-input NOR phase-splitter transistors have the largest geometries. The output NOR gates use a wire-or configuration which will lower the high-state transient output response. However, since these devices are not in the logic path of the internal flip-flops, they will not affect the memory loss threshold. The layout is symmetric between different storage cells.

State Vector Selection.—The response analysis shows that internal memory loss should occur at nearly the same level for all internal storage locations. The expected failure mode is zeros going to ones at the output. Memory loss failure should be independent of the G_R and R_B (read) connections, but will be affected by the write logic signals. A low G_W level activates the write circuitry, and is expected to be the most sensitive condition. Thus, the state vector for upset testing should correspond to stored zeros with the write enable pulse low. Timing sensitivity is determined by varying the timing of the radiation pulse to overlap the write enable period of the various storage cells.

Functional Testing.—A functional test of this circuit requires that it be in the read mode. The functional test consists of reading the output a short time period after the radiation pulse, comparing it to the written pattern.

4-2 DIELECTRICALLY-ISOLATED DEVICES.

4-2.1 General Considerations.

Response Mechanisms.—The response mechanism of the dielectrically-isolated circuits is expected to be secondary photocurrent in the output transistor. The output transistor has the largest geometry and also relatively large external base-emitter resistance paths. A topological view of a typical Schottky transistor used in these circuits is shown in Figure 10. It has an area that is approximately four times that of the internal phase splitter transistors. A significant amount of the collector area is taken by the Schottky diode and n^+ tunnel. The typical base area is 4×10^{-5} cm^2.

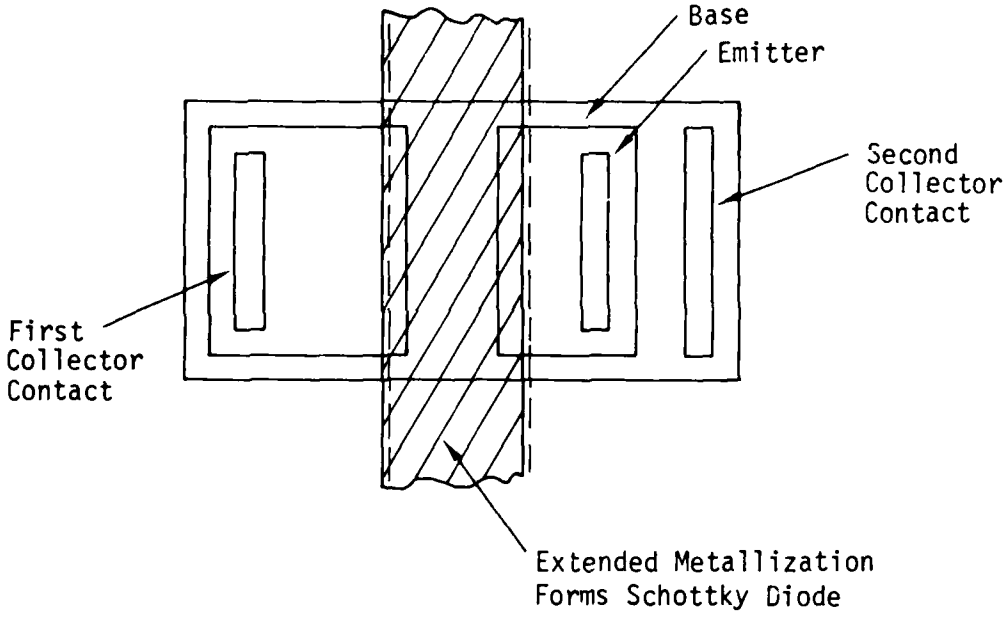


Figure 10. Typical output transistor geometry for the 1276 and 1284 dielectrically isolated circuits.

Primary Photocurrent Calculation.—The primary photocurrent of the dielectrically-isolated devices cannot be directly calculated from equations 1 through 4 because of the finite collector tub depth that limits the available charge volume. Since the lifetime is $\sim$ 1 μs, the diffusion length is $\sim$ 60 μm, and much of the collector tub volume will be collected as primary photocurrent. Assuming that the collector tub depth is 8 μm, and adding a factor of 2 to the base area to allow for lateral collection of carriers, the normalized primary photocurrent is 4×10^{-14} $\frac{\text{A-s}}{\text{rad(Si)}}$. This estimate could be in error by as much as a factor of 4 because of uncertainties in the assumptions that are the basis of the calculation.

Estimated Response Threshold.—The basic output logic cells used in the two dielectrically-isolated circuits use an external base-emitter resistor of 3K. If we assume that secondary photocurrent occurs when V_{BE} reaches 0.6 V, the response threshold is about 1.4×10^{9} rad(Si)/s. This is less accurate than the estimate of the thresholds of the junction-isolated devices because, as discussed in the previous paragraph, the primary photocurrent depends on variables other than the surface area. Variations in h_{FE} will also have some effect on the turn-on threshold, and in general one expects larger unit-to-unit variations in the threshold of devices that respond because of secondary photocurrent.

Several different logic cell design variations are used in these circuits. However, their base-emitter resistance paths are usually lower than that of the output cell. The area of all internal transistors is much less than the output transistor, leading to the conclusion that the output cell has the lowest threshold for both D.I. circuits.

4-2.2 477-1276 4-Bit Counter

Response Analysis.—As shown in the logic diagram of Figure 11, the 477-1276 counter is functionally very similar to the 54193. Examination of the topology and logic cell designs shows that all four internal flip-flops have similar topological designs. The flip-flops are connected to the Q and $\bar{Q}$ outputs through steering diodes, and will lose information when either the internal cells or outputs turn on. The logic cell analysis discussed earlier shows that the output cell is the most sensitive. Internal storage loss is expected to occur when the output transient exceeds the noise margin of the internal storage cell; the transition point is about 2.1 volts because of the diode steering logic.

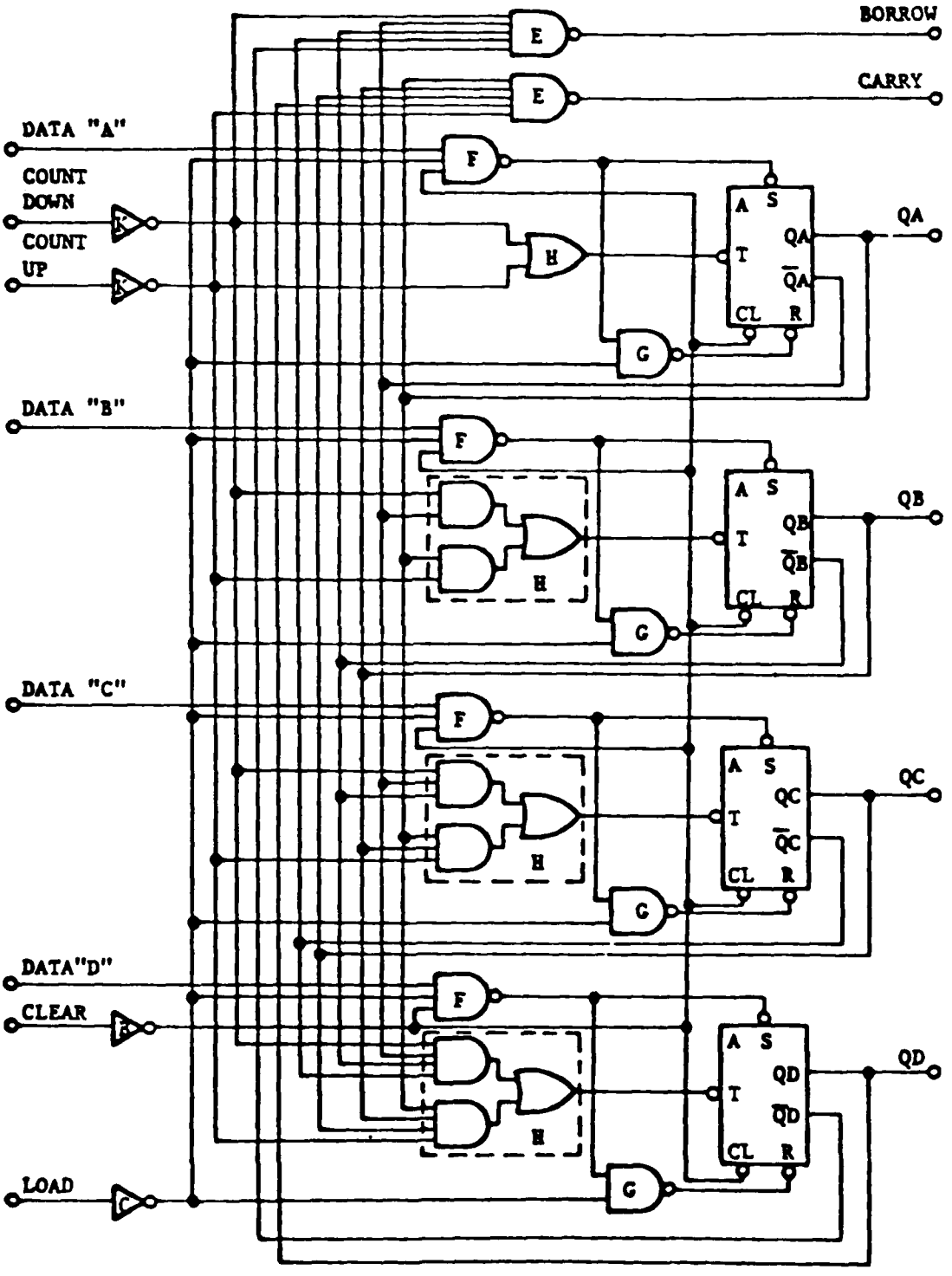


Figure 11. Logic diagram for the 477-1276 counter.

State Vector Selection.—The topological analysis showed that all four bits are similar in design, and should be equivalent from the standpoint of upset response. All four outputs can be examined after the radiation pulse, using state vectors that represent different logic states for all internal storage cells.

Functional Testing.—The same functional test used for the junction-isolated 54193 can be used for the 477-1276 counter.

4-2.3 477-1284 4x4 Register File

Response Analysis.—The logic diagram of the junction-isolated 74LS670 and dielectrically-isolated 477-1284 register files are identical, as shown in Figure 9. The output logic cell design is similar to that used in the 477-1276 counter, and is expected to upset at the same level. No significant geometrical differences were observed between outputs or between internal logic elements of common design.

State Vector Selection.—This device is expected to be most sensitive when the write mode is activated, so the state vectors selected during the radiation test must include this mode.

Functional Testing.—The same functional test is used for the 74LS670 and 477-1284 devices. All four outputs are examined after exposure in the write mode to determine the status of stored information.

SECTION 5
RADIATION TEST RESULTS

5-1 EXPERIMENTAL DETAILS.

5-1.1 Simulation Source.

All radiation testing was done using 15 MeV electrons from the Boeing linear accelerator. The radiation pulse width was 2 μs, which was sufficient to establish equilibrium conditions in the Schottky TTL devices. The beam area was restricted to minimize replacement currents from external wiring that might interfere with the output response. This was accomplished by using a collimator along with a reduction in the current of the accelerator.

A thin-film calorimeter[7] was used for dosimetry. A p-i-n diode was then used to monitor the pulse shape so that the dose rate could be determined.

5-1.2 Test Circuits and Instrumentation.

During radiation testing all circuit outputs were loaded with the network shown in Figure 3, simulating a worst-case fanout of 10 for each logic state. Special high input impedance line drivers were used to transmit the output response through terminated cables to oscilloscopes that recorded the transient output response. Power supply current signals were measured with a current transformer.

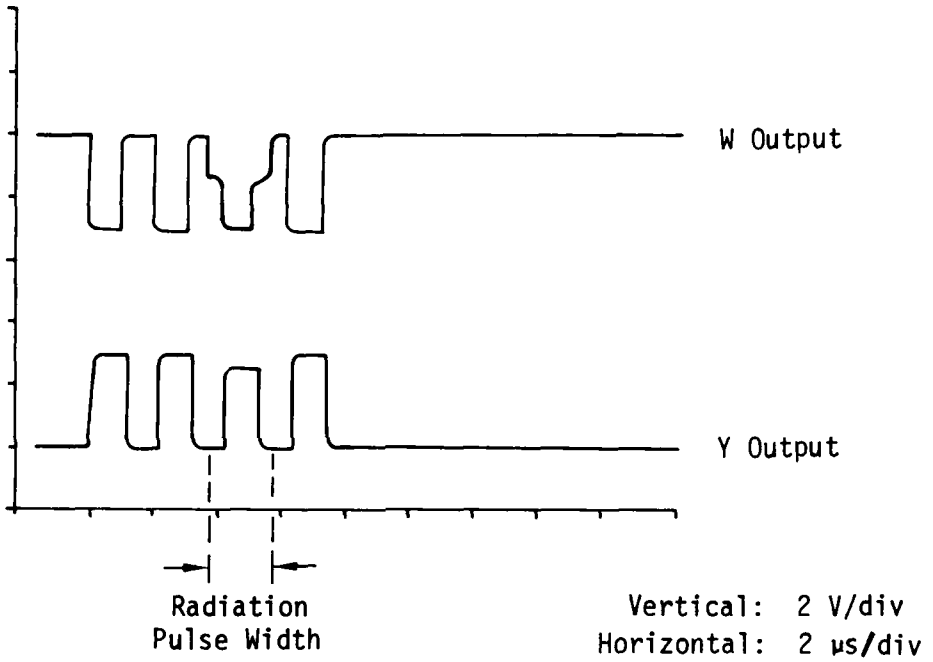
Input signals were provided by several pulse generators that provided TTL-compatible signals. These pulse generators were triggered synchronously with the radiation pulse; a special delay circuit allowed the radiation pulse position to be varied so that the edge sensitivity of the output response could be determined.

Functional testing was done with the same oscilloscope trace that recorded the device output. The input pulse timing was adjusted so that this functional test occurred a short time after the radiation pulse.

5-2 RESULTS FOR THE VARIOUS CIRCUITS.

5-2.1 54151 Multiplexer.

An example of the transient response of the 54151 multiplexer is shown in Figure 12. The output response follows the radiation pulse, and the output of the W output is about four times that of the Y output, as expected from the analysis. The pulse train in Figure 12 represents various inputs; the output did not depend on which input was selected as long as it was in the high state. As shown in the figure, there is no significant response when the outputs are low.



Note: Dose Rate = 3.8×10^8 rad(Si)/s

Figure 12. Transient output response of the 54151 multiplexer.

Five different units of this circuit were tested, and their response amplitudes agreed within about 10%. The transient threshold for a 200 mV response was 4.5×10^7 rad(Si)/s for the W output, and 2.9×10^8 rad(Si)/s for the Y output. This agreed closely with calculations of the response threshold, and shows the importance of internal device geometry in determining the upset response.

5-2.2 54193 Counter.

The 54193 counter exhibited the highest sensitivity to radiation when the most significant bit was high during irradiation. As discussed in Section 4-2.2, this was due to the larger size of the wire-or phase splitter transistor used in the OR gate that drives the MSB flip flop. The upset threshold of the five devices ranged from 1.7 to 1.9×10^8 rad(Si)/s when tested in this mode. The other outputs failed at about 2.5×10^8 rad(Si)/s, which is in excellent agreement with the difference predicted by the geometry of the phase-splitter transistors.

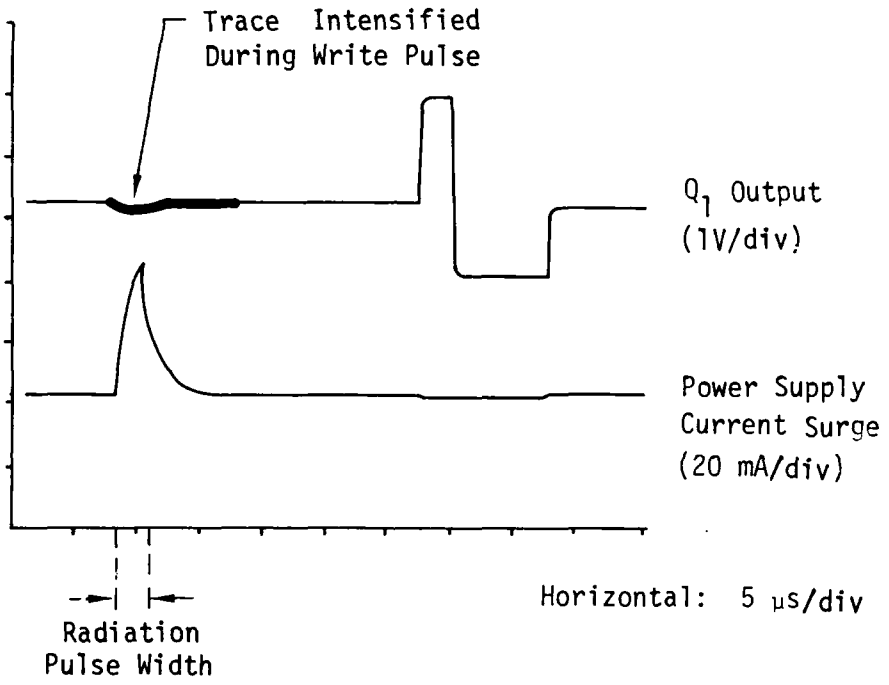
5-2.3 74LS670 Register File.

The typical output response of the 74LS670 register at the memory loss threshold is shown in Figure 13. The device is in the write mode while being irradiated (the intensified line shows the time period that the write pulse is enabled), and the radiation overlaps the input select pulse of one of the four inputs (the input is high). As shown in the functional test that occur afterwards, the first bit is no longer low, showing functional failure. The failure mode was always low going to high, as predicted by the analysis. No consistent differences were observed between different memory locations.

For the five units tested, the threshold for memory loss ranged from 2.5 to 3.4×10^7 rad(Si)/s. At levels about a factor of 2 higher, all internal cells lost memory, regardless of the time relationship between their input select signals and the radiation pulse.

The lower trace in Figure 13 shows the power supply current surge of this device. Since it is not gold doped, lifetimes of about 1 μs occur in the substrate, with a corresponding time response for the power supply surge (essentially substrate photocurrent).

The response of the 74LS670 agreed closely with the results of the analysis. Slightly larger unit-to-unit variations in response threshold occurred, but this is expected because of variations in lifetime between units.



Note: Dose Rate = 2.7×10^7 rad(Si)/s

Figure 13. Radiation-induced memory loss in the 74LS670 register file.

5-2.4 477-1276 Counter.

The typical radiation response of the 477-1276 counter at the counting loss threshold is shown in Figure 14. The upper trace shows the expected functional response to the input signals, while the bottom shows the loss of stored information in the most significant bit. This device was most sensitive to counting loss when the radiation pulse overlapped an internal clock transition. This was expected from the analysis. Note the change in the one state level prior to the transition.

Four different units were tested, and more variation was observed in their upset thresholds than for the junction-isolated circuits, as shown in Table 5. All internal bits failed at about the same level, provided that the radiation pulse overlapped the negative clock transition for the particular bit. As shown in the table, at slightly higher radiation levels the upset threshold was independent of the clock position.

Table 5. Counting loss threshold levels for the 477-1276 counter.

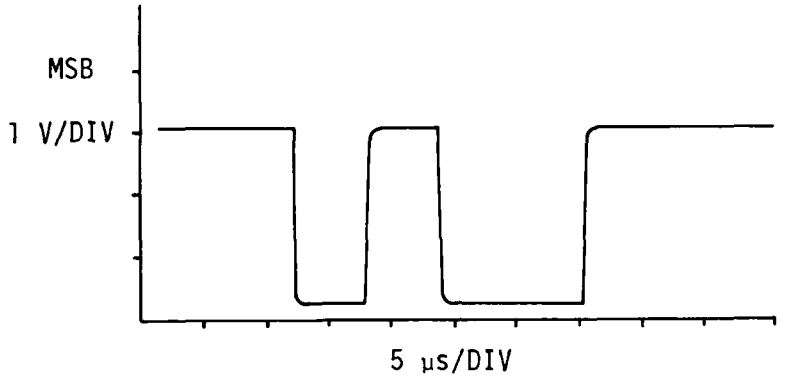
Unit	Position-Sensitive Threshold* [rad(Si)/s]	Position-Independent Threshold [rad(Si)/s]
131	2.7×10^9	3.5×10^9
132	1.5×10^9	2.2×10^9
133	2.2×10^9	2.4×10^9
134	1.9×10^9	2.4×10^9

*The radiation pulse overlapped an internal clock transition for position-sensitive thresholds. Position-independent thresholds caused counting errors when the pulse did not overlap the clock.

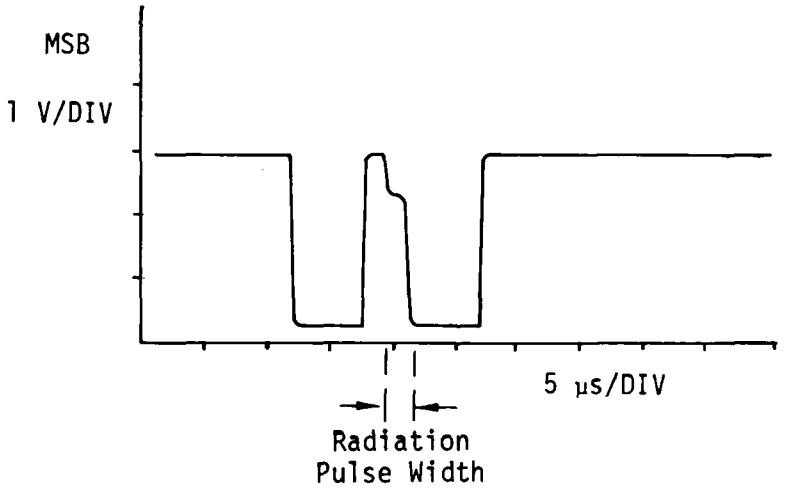
5-2.5 477-1284 Register File.

Because of the similar circuit function, the failure mode of the 477-1284 resistor file was virtually the same as that of its junction-isolated counterpart. However, it failed at levels about two orders of magnitude higher; this was anticipated from the analysis of the response mechanisms.

Table 6 shows the upset threshold levels for internal memory loss in this circuit (Q_2 output). Variations of about 10 were observed in the threshold of different internal storage cells. These differences appeared to be random between different units.



a) Normal Functional Response (no radiation pulse)



b) Functional Failure Induced by Radiation

Note: Dose Rate = 2.7×10^9 rad(Si)/s

Figure 14. Radiation-induced counting error in the most significant bit of the 477-1276 counter.

Table 6. Upset thresholds for internal storage cell loss in the 477-1284 counter.

Unit	Memory Loss Threshold [rad(Si)/s]
281	2.1×10^9
282	1.8×10^9
283	2.2×10^9
284	1.4×10^9

As expected from the analysis, this circuit was most sensitive when the write pulse was enabled during the time that it was exposed to the radiation pulse. It was tested in the same way as the 74LS670 that was discussed earlier.

5-3 DISCUSSION AND SUMMARY

These five circuit types were selected because they are good examples of basic classes and fabrication technologies used in MSI devices. There are MSI circuits with far more complicated functions, and the test results for this small number of devices undoubtedly does not encompass the range of behavior that can be found in MSI circuits. It is important to consider the mechanisms that were identified to cause variations in upset behavior so that the results can be extended to other device types and other fabrication technologies.

During the initial planning it was clear that relatively few examples of state vector sensitivity had been found, and that it was likely that many devices could be satisfactorily tested with abbreviated test methods (response Category I). Therefore, it is not surprising that three of the five devices did not show state vector sensitivity, other than the obvious synchronization requirements dictated by the basic circuit function. As shown in the summary in Table 7, two device types did show significant differences in the sensitivity of internal modes that were consistent between units (response Category II). Geometrical factors were the cause of this behavior, as verified by the close agreement between the radiation test results and the analysis.

Table 7. Summary of radiation test results

Device Type	Response Category	Upset Threshold [rad(Si)/s]	Technology (Response Mechanism)
54151 Multiplexer	II	4.5×10^7, output "W" 2.4×10^8, output "Y"	Standard Gold-Doped TTL (Substrate Photocurrent)
54193 Counter	II	$1.7 - 1.9 \times 10^8$, MSB $\sim 2.5 \times 10^8$, other bits	Standard Gold-Doped TTL (Substrate Photocurrent)
74LS670 Register File	I*	$2.5 - 3.4 \times 10^7$	Schottky TTL (Substrate Photocurrent)
477-1276 Counter	I*	$1.5 - 2.7 \times 10^9$	Dielectrically-Isolated Schottky TTL (Secondary Photocurrent)
477-1284 Counter	I*	$1.4 - 2.2 \times 10^9$	Dielectrically-Isolated Schottky TTL (Secondary Photocurrent)

*There are obvious functional requirements that determine basic synchronization requirements between clock or enable signals and the radiation pulse. These are not Category II devices because the response does not depend on the location of internal storage cells.

It must be kept in mind that these circuits are only examples, and that the identification and analysis of the mechanisms is the important point, not the magnitude of the effect. For example, although a relatively large difference was observed in the output sensitivity of the 54151 multiplexer, the difference in response sensitivity of the 54193 bits is less than a factor of 2, and might be considered unimportant for many applications. However, this circuit was selected with no a priori knowledge of the unusual phase-splitter transistor geometry. The important point is that internal design asymmetries exist that cause state vector sensitivity, and that they can be found by a relatively simple topological analysis.

No devices were found that fit response Category III. For junction-isolated devices this is not surprising because the response mechanisms involve junction area, lifetime and resistance values and it is unlikely that random differences among these factors could be large enough to cause large differences in the response. Since secondary photocurrent threshold levels were typically an order of magnitude higher, they will generally not be a factor for junction-isolated devices.

On the other hand, dielectrically-isolated devices respond because of secondary photocurrent, which is affected by gain, resistance values, and base-emitter voltage in addition to primary photocurrent. These variables have a greater likelihood of statistically combining to cause abnormally large secondary photocurrents, and one would expect that Category III devices would be more likely to occur in technologies that respond from this mechanism. For example, Figure 15 shows a distribution of upset response thresholds for an older generation of TTL NAND gates that were fabricated with dielectric isolation.[8] One device (about 1. of the population) responded at a level one order of magnitude below the mean failure level. This was caused by an open base-emitter resistor in the output transistor circuit. Surprisingly, this circuit passed all of the electrical requirements even at the Mil-Spec temperature extreme. This kind of mechanism could easily occur in internal logic cells of MSI devices, where it would be more difficult to detect with electrical measurements because of the isolation between the internal cells and the input and output leads.

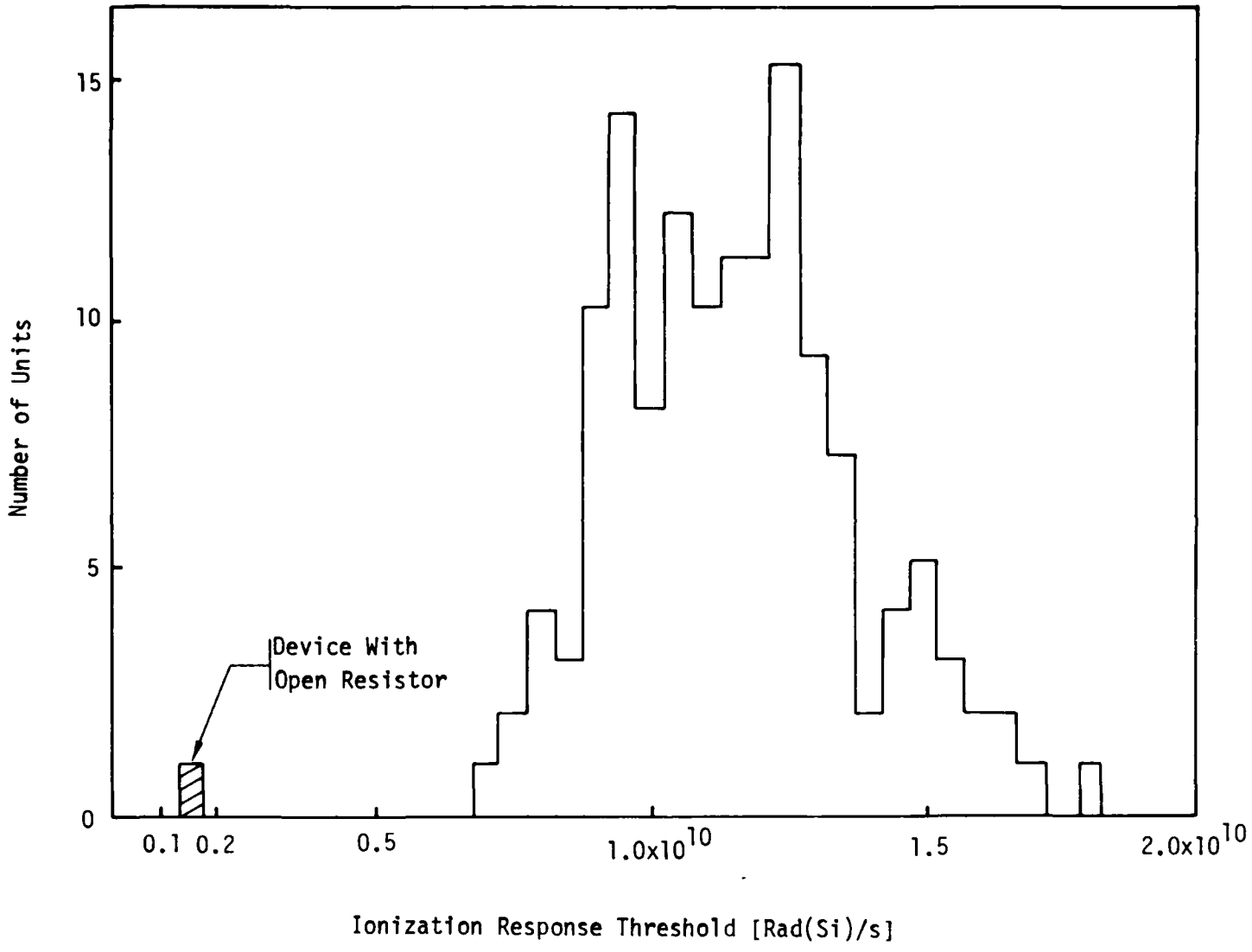


Figure 15. An example of category III behavior: Distribution of TTL inverter upset response thresholds (after reference 8).

SECTION 6
CONCLUSIONS AND DISCUSSION

6-1 RESULTS OF THE TTL STUDY.

The results of the TTL study have shown the importance of internal component geometry and chip layout in determining the upset response of the device. For example, the large geometry of the phase-splitter transistor of the 54151 multiplexer makes it extremely sensitive to transient upset. This sensitivity is only apparent at one of the two outputs, and could easily be missed by careless test methods that failed to consider the internal device geometry; the result would be overestimation of the upset response threshold level by about a factor of 4.

Internal device geometry was also important for the 54193 counter. One of the internal transistors had an unconnected input, with significantly larger area. This caused one of the internal storage bits to upset at a lower radiation level than the other three even though the logic design of all four bits was identical.

For three of the five device types tested, no unusually sensitive internal locations were found. This is not surprising, because most MSI devices are relatively simple in their functional design and use internal geometries and logic design methods that are similar to SSI logic. Similar design rules are used, and in most cases the internal designs are symmetric so that extreme differences in upset response levels are not observed between different operating modes. Most of the observed differences can be directly attributed to differences in junction area, and are easy to identify from a photomicrograph.

Most sequential circuits have complicated internal storage element configurations, and in general transient-induced changes in these registers are easily checked by functional testing. Of course, the functional test must be carefully planned to verify proper operation after irradiation. In a sense, it is easier to detect transient failures in sequential logic circuits because the proper operation of many different storage cells are verified each time that the device is tested. For combinational circuits, individual input and output state vectors have to be considered.

6-2 EXTENSION TO OTHER DEVICE TECHNOLOGIES.

In principle the same analysis methods can be applied to other technologies such as CMOS, I^2L, and ECL. However, their response mechanisms can differ; for example, CMOS devices have large parasitic transistor gains, requiring more complicated analysis (the latchup sensitivity of this technology requires similar analyses). It seems unlikely that other junction-isolated technologies could have highly sensitive operating modes that did not involve obvious differences in device geometry or logic cell layout. Thus, the topological analysis is expected to provide similar insight into their sensitive response locations.

Relatively few MSI functions are available at the present time in either ECL or I^2L, and less is known about their response mechanisms. Careful analysis of the response of simple structures should allow the same technique used for TTL devices to be applied. When planning topological analyses, it is important to keep in mind that the analysis must consider all of the failure modes in order to be valid. Clearly, details such as substrate interactions and the presence of parasitic junctions under metallization or crossunders are extremely important when considering less familiar digital structures.

It is also useful to examine the limited test data available on LSI devices. Most testing has not revealed particularly sensitive modes, although the crossunder sensitivity reported for the SBP9900 is an exception.[4] At this point the LSI technology appears to be similar to MSI; most devices do not exhibit asymmetries in their response, but there are a few exceptions that can only be identified by fortuitous or complete testing, or by a combination of testing and analysis. This is probably the result of designing circuits with basic logic blocks that replicate geometries and obey stringent electrical design rules. This prevents unusual geometries in most cases.

6-3 PERSPECTIVE.

Since the basic mechanisms that control the upset response of digital devices involve the device geometry and chip layout, it is logical to require that a topological examination be included as part of any upset response standard. The analysis method included in the present standard is straightforward to apply, and does not require detailed processing information from the manufacturer. It was selected as a compromise between the extremes of an involved, research-oriented analysis and an overly simplified approach that ignores the device topology. This

seems to be a reasonable approach, but it must be recognized that the majority of MSI devices tested to date have not been subjected to such an analysis. It must also be admitted that in many cases simplified "trial and error" approaches are satisfactory. This is a consequence of the logic cell approach that is used for most present-day circuits.

The analysis is not needed for all device types. However, there is no a priori method of determining whether a topological analysis is needed, and the results for the five devices tested in this study show the importance of internal device geometry in determining the relative upset threshold of internal locations. The test standard must certainly include an examination of the basic reasons for the device response if it is to have any hope of identifying sensitive modes for arbitrary devices.

One can speculate that future devices will depart more drastically from the simple extensions of basic cells that are used for current technology MSI devices, which will increase the importance of the analysis. There are already examples of mixed technologies, such as TTL memories that consist of ECL memory cells with TTL interface circuitry. One would expect more innovative design solutions in the future that take advantage of the low node capacitance and higher noise immunity of internal circuits; these designs will undoubtedly differ in their radiation behavior from present designs, and will require careful analysis of fundamental response mechanisms before the topological analysis is applied.

SECTION 7

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APPENDIX

MIL-STANDARD TEST METHOD

This appendix contains a copy of Draft 2 of the Mil-Standard test method that was developed for upset threshold response testing.

1. PURPOSE AND SUMMARY

The purpose of this test procedure is to define a method to measure the upset response threshold of MSI digital integrated circuits that are exposed to pulses of transient ionizing radiation. The method consists of an analysis of the electrical design and topology of the circuit to determine its most sensitive operating conditions, followed by radiation testing in an appropriate simulation facility. In order to determine the upset threshold it is necessary to use a sequence of pulses at various dose rates. The upset threshold is then determined by successive approximation.

The method emphasizes ways to minimize the number of different conditions under which an MSI device must be tested, since cost and radiation damage restrict the number of radiation pulses that can be used.

1.1 Definitions

Special terms used in this test method are defined below:

a. MSI Integrated Circuit

An integrated circuit with a total number of internal components that is equivalent to the number of components in 15 to 100 NAND gates. MSI stands for medium scale integration. Examples of MSI circuits are shift registers, counters, small memories, and decoders.

b. Combinational Logic

A digital logic system with the property that its output state at a given time is solely determined by the logic signals at its inputs at the same time (except for small time delays caused by the propagation delay of internal logic elements). Note that combinational circuits contain no internal storage elements. Examples of combinational circuits include multiplexers, decoders, and gate arrays.

c. Sequential Logic

A digital logic system with the property that its output state at a given time depends on the sequence and time relationship of logic signals that were previously applied to its inputs. Examples of sequential logic circuits include shift registers, counters, and arithmetic logic units.

d. State Vector

A state vector completely specifies the logic condition of all elements within a logic circuit. For combinational circuits the state vector includes the logic signals that are applied to all inputs; for sequential circuits the state vector must also include the sequence and time relationship of all input signals. In this standard the output states will also be considered part of the state vector definition.

For example, an elementary 4-input NAND gate has 16 possible state vectors, 15 of which result in the same output condition ("1" state).

A 4-bit counter has 16 possible output conditions, but many more state vectors because of its dependence on the dynamic relationship of various input signals.

e. Upset Response

The electrical response of a circuit when it is exposed to a pulse of transient ionizing radiation. Two types of upset response can occur:

(1) responses that are caused by a combinational logic chain that spontaneously recover to the initial logic state vector after irradiation, and

(2) responses that are caused by a change in one of the internal storage cells, changing the state vector of the circuit. Because the radiation changes the state vector, the circuit spontaneously recovers to a different logic state. The circuit can be restored to its original state vector by reinitialization after irradiation.

Although the term upset response is usually used to describe output voltage responses, some devices—such as open collector gates—are better characterized by measuring the output current. Upset response

must also include the transient currents that are induced in the power supply lead as well as the response of the device inputs, although in most applications the input response is not significant.

f. Response Categories

Experience with SSI devices has shown that although a circuit is usually most sensitive to logic upset in one of its logic states (generally the "1" state), the upset threshold of the circuit is nearly always the same for state vectors that result in the same output logic state. Thus, a 4-input NAND gate has the same upset threshold regardless of which of the 15 state vectors are selected that result in a "1" output state. This occurs because (1) the inputs are usually not directly involved in the upset response mechanism, and (2) there is a high degree of symmetry in the layout and logic cell design of the circuit.

For MSI devices, it is useful to define three different categories of devices in terms of their internal design and radiation response mechanisms:

Category 1—Devices with the same symmetry in design and response exhibited by SSI devices so that there are no hidden state vectors with unusually low response thresholds. The selection of state vectors for Category 1 devices can be made from a logic cell analysis, based on response mechanisms of SSI devices.

Category 2—Devices with internal logic cells that are unusually sensitive to transient ionization because of differences in geometry or circuit design. These differences are consistent for different units (as long as the same mask set was used in fabrication), and can be identified by topological analysis.

Category 3—Devices with internal logic cells that are unusually sensitive to transient ionization because of random variations in processing. These locations vary between different units, and in general cannot be identified by analysis. Radiation testing with a large number of state vectors is the only sure way to detect Category 3 devices.

Most MSI devices are in Category 1. Examples of Category 2 devices include circuits with internal logic cell asymmetries (such as "wire-or" inverters with unused sections) or tunnels used as metallization crossunders that change the response of specific cells. Although no Category 3 devices have been specifically identified, a potential example is a memory with an internal defect (such as an emitter spike) that causes one location to have a low upset threshold.

1.2 Interferences

There are several interferences that need to be considered when this test procedure is applied. These include:

a. Total Dose Damage

MSI devices may be permanently damaged by total dose, which limits the number of radiation pulses that can be applied during transient upset testing. The total dose sensitivity depends on the fabrication techniques and device technology.

b. Dosimetry Accuracy

Since this test method ultimately determines the dose rate at which upset occurs, dosimetry accuracy inherently limits the accuracy of the method.

c. Latchup

Some types of integrated circuits may be driven into a latchup condition by transient radiation. If latchup occurs, the device will not function properly until power is temporarily removed and reapplied. Permanent damage may also occur. Although latchup is an important transient response mechanism, this procedure is not applicable to devices in which latchup occurs.

1.3 Other Applicable Standards

Several test standards are applicable to this test method. These include:

a. Calibration of Absorbed Dose from Gamma or X Radiation (ASTM E666-78).

b. Standard Recommended Practice for the Application of Thermoluminescent Dosimetry (ASTM E668-78).

c. Steady State Total Dose Irradiation Procedure (MIL-STD-883B, Method 1019.1).

d. Dose Measurement for Use in Linear Accelerator Pulsed Radiation Effects Tests (ASTM F-526).

2. APPARATUS

The equipment required for this method includes an electrical schematic, a photomicrograph or composite mask drawing of the device, a transient radiation simulation source, dosimetry equipment, and electrical equipment for the measurement of the device response and functional testing. A test plan is also required. The test plan must specify the following:

(a) the pulse width, energy, and type of radiation source;
(b) the voltage and electrical loading conditions on each pin of the device during testing;
(c) the resolution and accuracy required for the upset response threshold of individual devices, along with the successive approximation method used to vary the radiation level;
(d) the failure criterion for transient logic failure; and
(e) the functional test to be made after irradiation.

The state vectors in which the device is to be irradiated are determined from the design and topological analysis of the circuit and thus are not part of the initial test plan.

2.1 Items Required for the Device Analysis

2.1.1 Electrical Schematic

A schematic diagram of the device to be tested.

2.1.2 Photomicrograph or Mask Drawing

A photomicrograph or composite mask drawing of the test device that allows the identification of isolation and diffusion regions, and quantitative comparison of junction areas.

2.2 Radiation Simulation and Dosimetry Apparatus

2.2.1 Transient Radiation Simulation Source

A pulsed high energy electron or bremsstrahlung source that can provide a dose rate in excess of the upset response threshold level of the device being tested at the pulse width specified in the test plan. In general a linear accelerator (linac) with electron energies of 10 to 25 MeV is required, although in some instances a flash x-ray with charging voltages above 2.5 MV may be satisfactory.*

2.2.2 Total Dose Dosimetry System

A dosimetry system such as a TLD (thermoluminescent dosimetry system) or calorimeter that can be used to measure the total absorbed dose produced by a single pulse of the radiation source.

2.2.3 Pulse Shape Monitor

A device for monitoring the shape of the radiation pulse such as a p-i-n diode. In some instances it may be possible to directly determine the pulse shape by measuring the total beam current of the accelerator with a current transformer.

2.2.4 Active Dosimetry Standard

An active dosimeter that allows the dose rate to be determined from electronic measurements. This may be a p-i-n detector, a Faraday cup, or a combination of a calorimeter and current transformer.

2.3 Electronic Test Equipment

2.3.1 Radiation Test Fixture

A test fixture that allows the device to be placed in the radiation beam with convenient connection to external equipment (pulse generators, power supplies, line drivers) required for testing.

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*The absorption coefficient of photons in silicon and packaging materials is relatively flat at energies above 2 MeV, and has a nearly constant ratio to the absorption coefficient of typical dosimetry systems. At lower energies absorption coefficients increase, which can introduce large dosimetry errors if the peak energy of a bremsstrahlung source is below 2.5 MeV.

2.3.2 Line Drivers

Line drivers that provide high input impedance to the device under test and can drive the low impedance of terminated output cables with adequate signal fidelity. The line drivers must be designed so that their own response to transient ionizing radiation is much smaller than that of the circuit being measured.*

2.3.3 General Purpose Test Equipment

Power supplies, pulse generators, cables, and termination resistors that are required to bias the device and establish its internal operating conditions.

2.3.4 Transient Response Measuring Device

An oscilloscope or transient digitizer that is used to measure the transient response of the device under test. The bandwidth and sensitivity of this equipment must be compatible with the pulse width and measurement criteria in the test plan. For extremely narrow pulses (< 20 ns) it may be necessary to correct the measured response for the distorting effect of the limited instrumentation bandwidth.

2.3.5 Functional Test System

A system that is set up to test the functional operation of the device under test while it is in the radiation test fixture. This may consist of (1) general-purpose equipment such as pulse generators and oscilloscopes or logic analyzers, (2) a commercial integrated circuit test system, or (3) a custom test fixture. The specific requirements of the functional test system depend on the specifications and requirements of the device under test, and are included in the test plan.

2.3.6 Temperature Measuring Equipment

A thermometer, calorimeter, or other temperature measuring device that can measure the ambient temperature of the device with an accuracy of at least $\pm$ 3°C.

*Although line drivers are normally not placed in the direct radiation beam, there is always some stray radiation that may affect the line driver. Furthermore, replacement currents in the wiring that connects the line driver to the circuit under test may also introduce a spurious response.

3. PROCEDURE

The procedure will be governed by a test plan that describes the device operating conditions, upset response criteria, functional test method, and radiation source requirements (see section 2). The procedure is divided into three parts: (1) analysis of the integrated circuit response mechanisms and geometry; (2) calibration and adjustment of the radiation facility; and (3) measurement of the radiation level at which transient upset occurs. The state vectors selected for irradiation are determined from the analysis step.

The test results are incorporated into a test report that includes necessary information about the test sample and measurement conditions as well as the test data.

3.1 Analysis

The purpose of the analysis step is to select the state vectors in which the device is most sensitive to transient upset so that they can be included in the set of state vectors used for testing. The analysis starts with the schematic diagram and a photomicrograph or composite mask drawing of the integrated circuit. It is assumed that the basic response mechanisms of the device are known from experience or test data on SSI devices fabricated with the same basic technology. Specific steps in the analysis are listed below.

3.1.1 Functional Block Analysis

Partition the circuit into functional logic blocks. Determine the logic path for each output, and identify similar internal functions. For example, a 4-bit counter can be separated into control, internal flip-flop, and output logic cells. There are four identical logic paths corresponding to each of the four bits. Upset mechanisms can then be associated with each block in the logic path.

3.1.2 Determine Relative Response Sensitivity

Measure the relative junction areas of critical transistors in each logic path. For devices that respond because of substrate photocurrent, the area of the isolation diffusion is measured, whereas for devices that respond because of secondary photocurrent, the base area is measured.

Assuming that the photocurrent at a specific radiation level is proportional to junction area, use nominal resistor values to determine the relative voltage drop (and hence the relative upset level) of each functional block in the logic path. This step will identify the logic element which has the highest sensitivity to radiation for each logic path. It also determines which internal logic state is most sensitive to transient ionization.

3.1.3 Identification of Asymmetries and Parasitic Junctions

Carefully examine the geometry of functionally similar logic paths to determine if any asymmetries exist that would cause specific locations to be more sensitive to upset. In order for such differences to be significant, an obvious difference in junction area must occur. Also examine the layout to check for tunnels or proximity to other elements that differ between functionally identical logic cells. Regions with obvious physical differences should be identified and included in the state vector set used for irradiation.

3.1.4 State Vector Selection

Use the results of the functional block analysis and topological analysis to select state vectors that correspond to the most sensitive logic cells.

3.1.5 Test Plan Modification

Use the results of the preceding steps to determine the response category of the device (Category 1 or 2) and incorporate the test vectors selected in step 3.1.4 into the test plan. The total number of state vectors selected for radiation testing must be compatible with cost and total dose limitations.

3.2 Setup and Calibration of the Radiation Facility

3.2.1 Accelerator Setup

Adjust the accelerator to the energy, pulse width and nominal intensity specified in the test plan. Verify that the beam area and uniformity are adequate for the device being tested and the placement of the active dosimeter.

3.2.2 Calibration

Measure the total dose and pulse width of the accelerator, using the TLD or calorimeter and an appropriate pulse shape monitor. ASTM methods E666-78 and E668-78 provide appropriate test methods.

3.2.3 Active Dosimeter Calibration

Calibrate the active dosimeter using the same methods. Verify that the active dosimeter has a linear response over the expected range of radiation levels.

3.2.4 Noise Test

Set up the radiation test fixture. Place small dummy load resistors on each pin of the test fixture that are nominally equal to the active impedance of each pin of the device (electrical measurements or circuit analysis can be used to determine the appropriate load impedances). Irradiate the test fixture and dummy loads and measure the output response. This response must be less than 1/3 of the output response that constitutes transient failure (see the test plan).

3.3 Radiation Testing

3.3.1 Sample Selection

The number of devices to be tested shall also be specified by the test plan. They should be randomly selected from the parent population (unless otherwise specified) and must be fabricated with the same mask set used in the analysis (3.1). Each part shall be individually identified with a serial number. For devices that are sensitive to damage from static discharge, appropriate handling methods must be used. In addition to the test devices, a minimum of two expendable devices shall also be selected from the test sample for use in setting up the functional test and transient upset equipment.

3.3.2 Set Up and Check Out Functional Test System

Assemble the equipment required for functional testing and adjust the waveform amplitudes and timing to the values specified in the test plan. Adjust the power supplies required for testing to the correct values and connect them to the radiation test fixture. Temporarily turn

off or disconnect the power and insert one of the expendable devices in the test fixture. Reapply power and verify proper operation of the functional test system.

3.3.3 Set Up and Check Out Upset Response Test System

Assemble the equipment required to measure the transient response of the device (this usually includes line drivers). Terminate all coaxial cables with their characteristic impedance. Place the active dosimeter in close proximity to the device under test (the beam uniformity was previously established in section 3.2). Place one of the expendable devices in the test fixture and set it up in the state vectors that were selected in section 3.1. Pulse the accelerator and measure the transient response of the device and the dose rate. If the response is greater or less than that defined as logic failure, adjust the accelerator for a higher or lower dose rate and repeat the test. Continue this process until the upset response level has been bracketed.

3.3.4 Determine Pulse Synchronization Effects

Change the position of the radiation pulse with respect to active electrical signals (such as a clock or memory write signal) to determine the most sensitive timing relationship between the radiation pulse and electrical input signals. Modify the test plan to include these synchronization requirements if significant differences are found. (This is usually necessary only for sequential logic circuits.)

3.3.5 Total Dose Damage Sensitivity Estimation

Calculate the total dose from a single pulse at the failure threshold level determined for the expendable device in step 3.3.3. Estimate the total dose damage threshold* from test data on similar device types or experiments. If the total dose per pulse exceeds 1% of this estimated threshold, then the devices must be tested before and after irradiation to determine the effect of total dose damage. If the total dose per pulse is less than 1% of this threshold level, total dose testing is not required.

*The total dose damage threshold is the level at which significant degradation—typically a 10% change—in electrical parameters occurs.

3.3.6 Total Dose Testing (Optional)

If the results of the previous step show that total dose testing is required, then each device must be electrically characterized before and after upset response testing. This testing must be compatible with MIL-STD-883B Method 1019.1, except that in this case a pulsed radiation source is used. (Although a separate experiment could be done with a steady-state source, this is not necessary. The only purpose of characterization is to directly determine the total dose damage that results from the pulsed irradiation used for upset testing.)

3.3.7 Radiation Testing of Serialized Devices

Turn off or disconnect the power and logic signals from the radiation test fixture. Before beginning the tests, measure the ambient temperature. Insert one of the serialized devices into the test fixture. Reapply power and logic signals from the functional test system and test the functional operation of the device in the test fixture. Establish the correct state vector, pulse the accelerator and measure the transient response. Also measure the dose rate using the active dosimeter. Functionally test the device after irradiation to determine changes in the state vector.

If the results of the test show that the response is below the upset failure criterion, increase the dose rate by the factor specified in the test plan and repeat the test.

Conversely, if the results show that the device is above the upset threshold, lower the dose rate by the factor specified in the test plan. Continue this sequence until data above and below the upset threshold are obtained within the interpolation range specified in the test plan. Keep track of the number of pulses and total dose and make sure that the total dose accrued during testing is well below the damage threshold of the device.

Repeat this sequence for each specified state vector. Additional units are tested in the same way, starting at the best estimated radiation level in order to minimize the number of pulses required in the test sequence.

3.3.8 Calculation of the Upset Response Threshold

For each device and state vector, determine the upset response threshold from dose rate data above and below threshold as determined with the active dosimeter. For upset responses that do not involve state vector changes interpolation can be used because the response is approximately proportional to the dose rate near the threshold level. For responses that involve state vector changes it is usually not possible to use interpolation; the accuracy of the result is then limited by the difference between successive radiation levels which bracket the upset response threshold.

3.4 Report

The report shall include device identification (including date or lot code), results of the device analysis, date of test, name of operator, type of test facility, pulse width, bias conditions, state vectors used for testing, upset criteria, test temperature, and the dose rate at which the upset response was identified for each logic state vector. Any additional data specified in the test plan must also be included.

4. SUMMARY

The following shall be specified prior to the start of the test program:

a. Device type, manufacturer, date code, mask identification, and the number of units to be tested.

b. Upset response criteria (including the output loading configuration).

c. Bias conditions.

d. Output pins to be measured.

e. Functional test requirements.

f. Input state vectors used for upset response testing.

g. Energy, pulse width and type of radiation simulation source.

h. Restrictions on total dose.

i. Ambient temperature range during testing.

j. Sequence used to adjust the dose rate in order to determine the upset threshold by successive approximation.

k. Interpolation or analysis method used to determine the upset threshold.

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